

Fig.1
(PRIOR ART)

Fig. 2 (PRIOR ART)

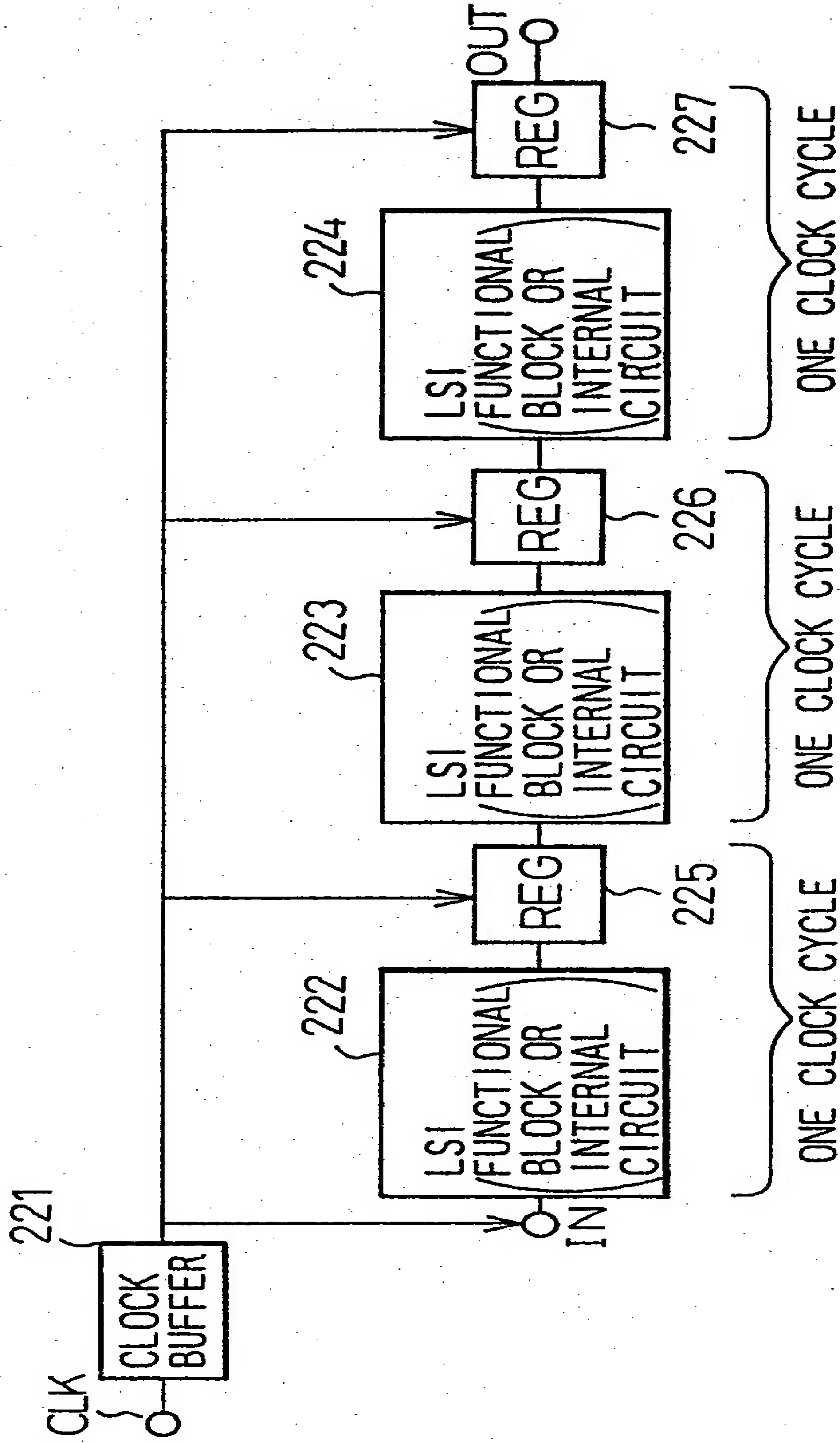


Fig. 3(PRIOR ART)

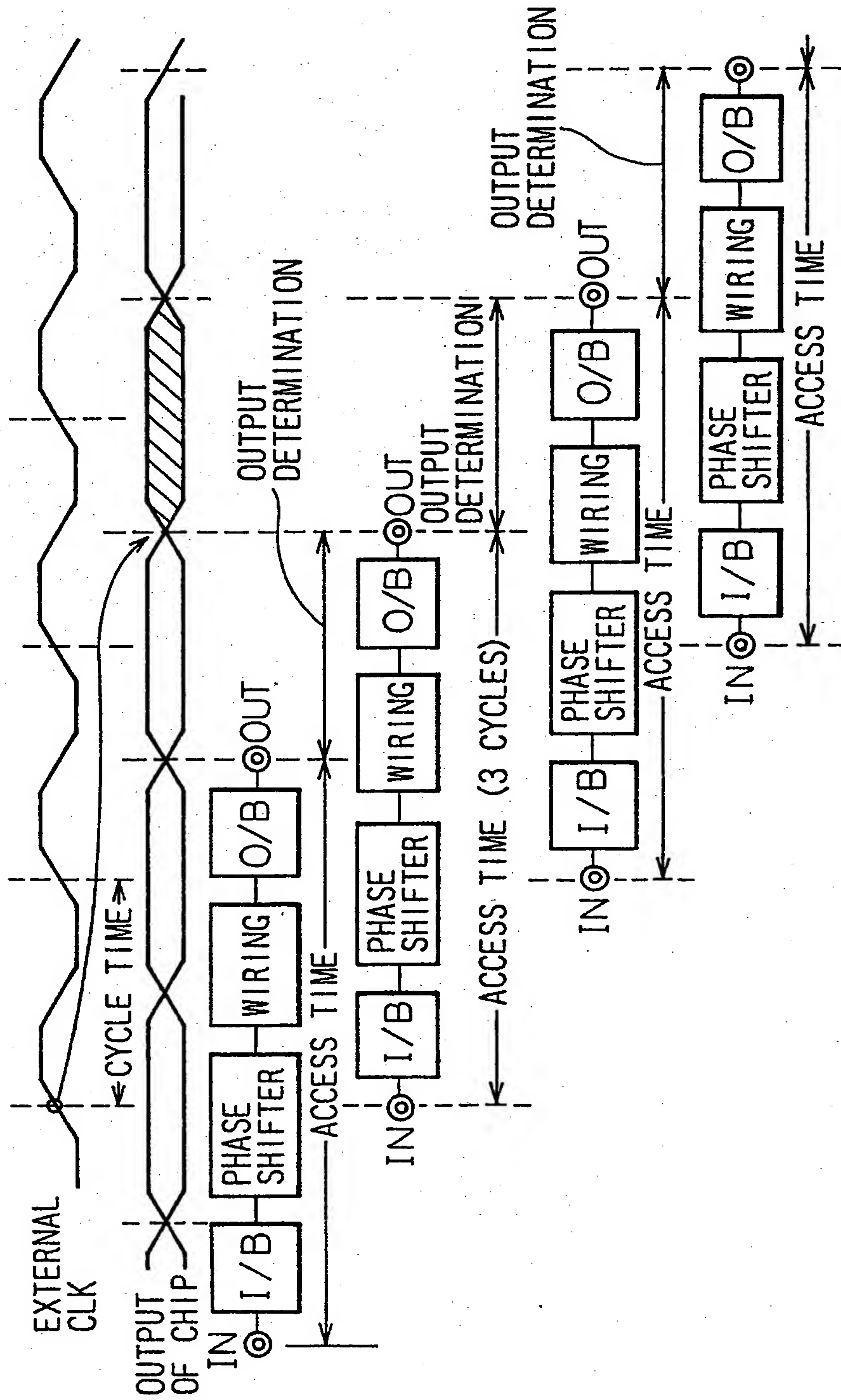


Fig. 4

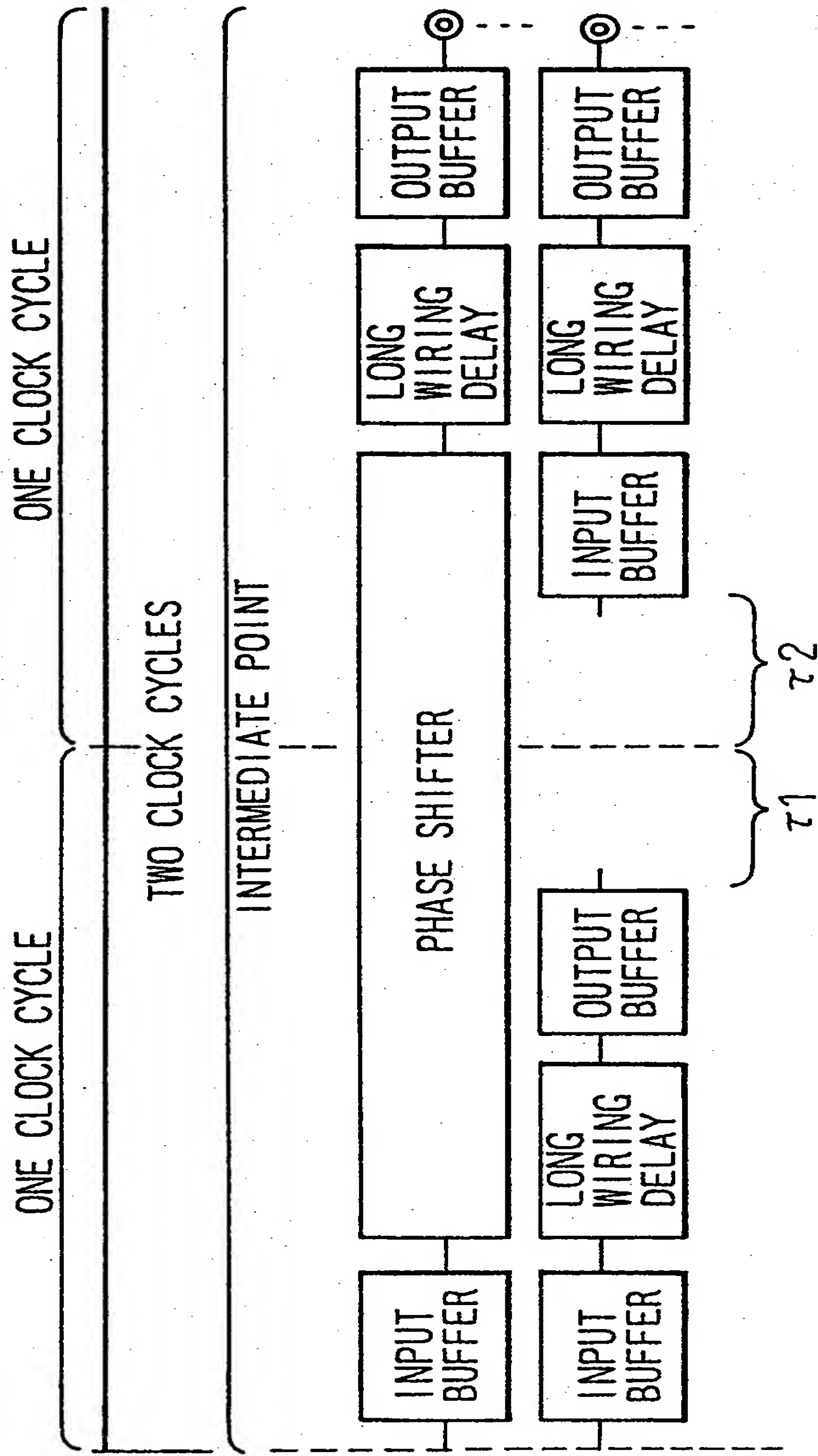


Fig 5

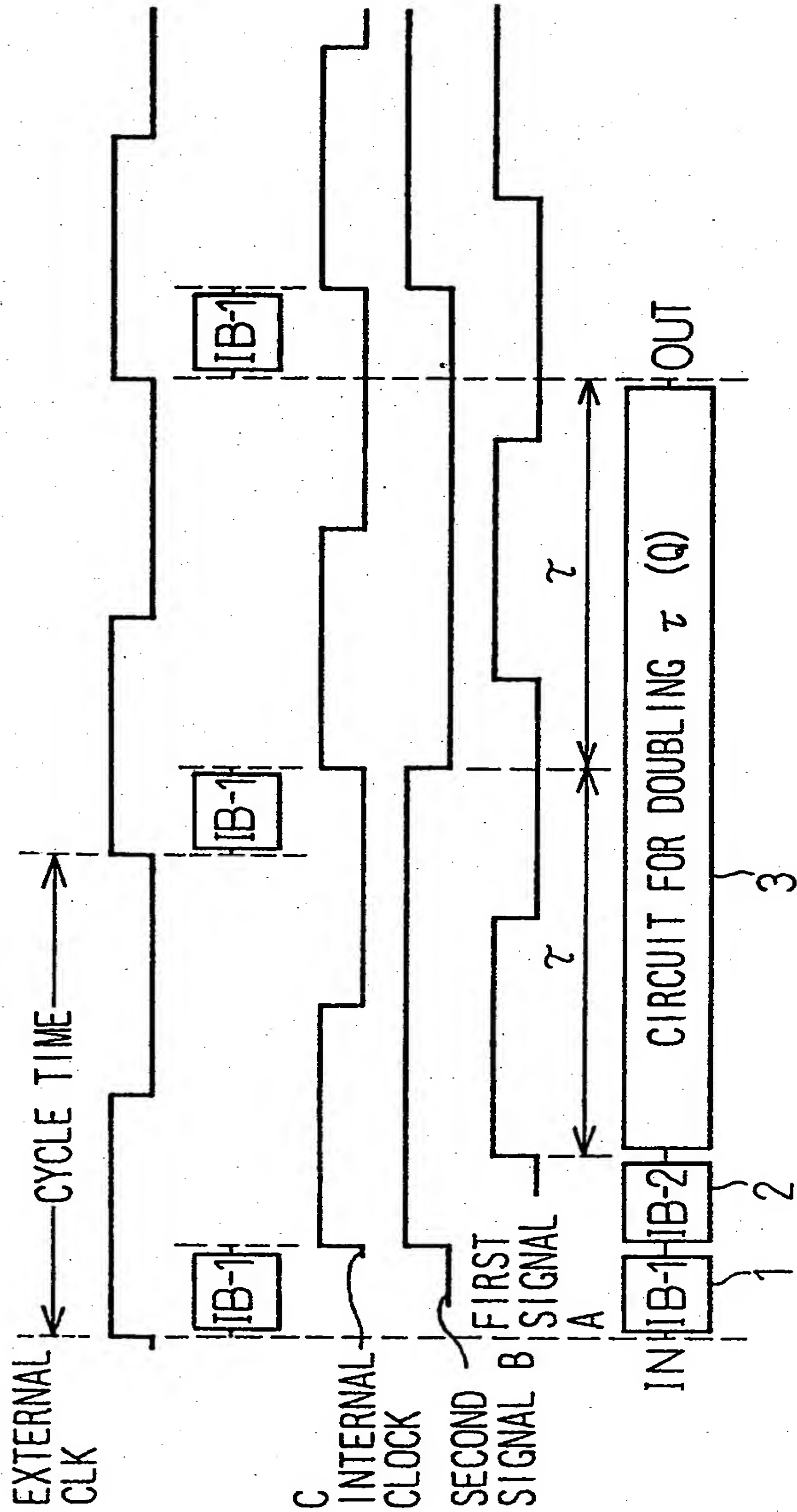


Fig. 6

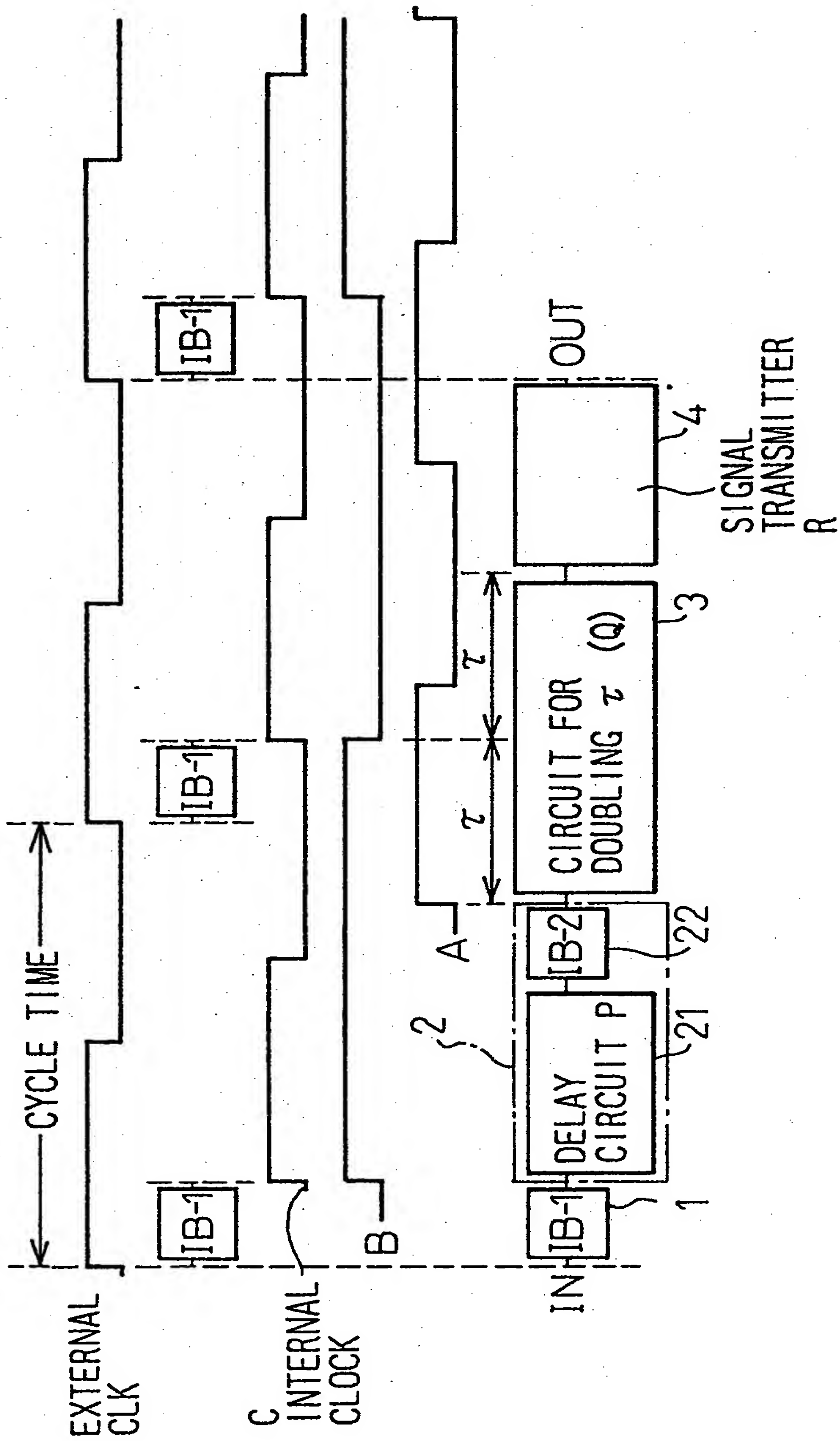


Fig. 7

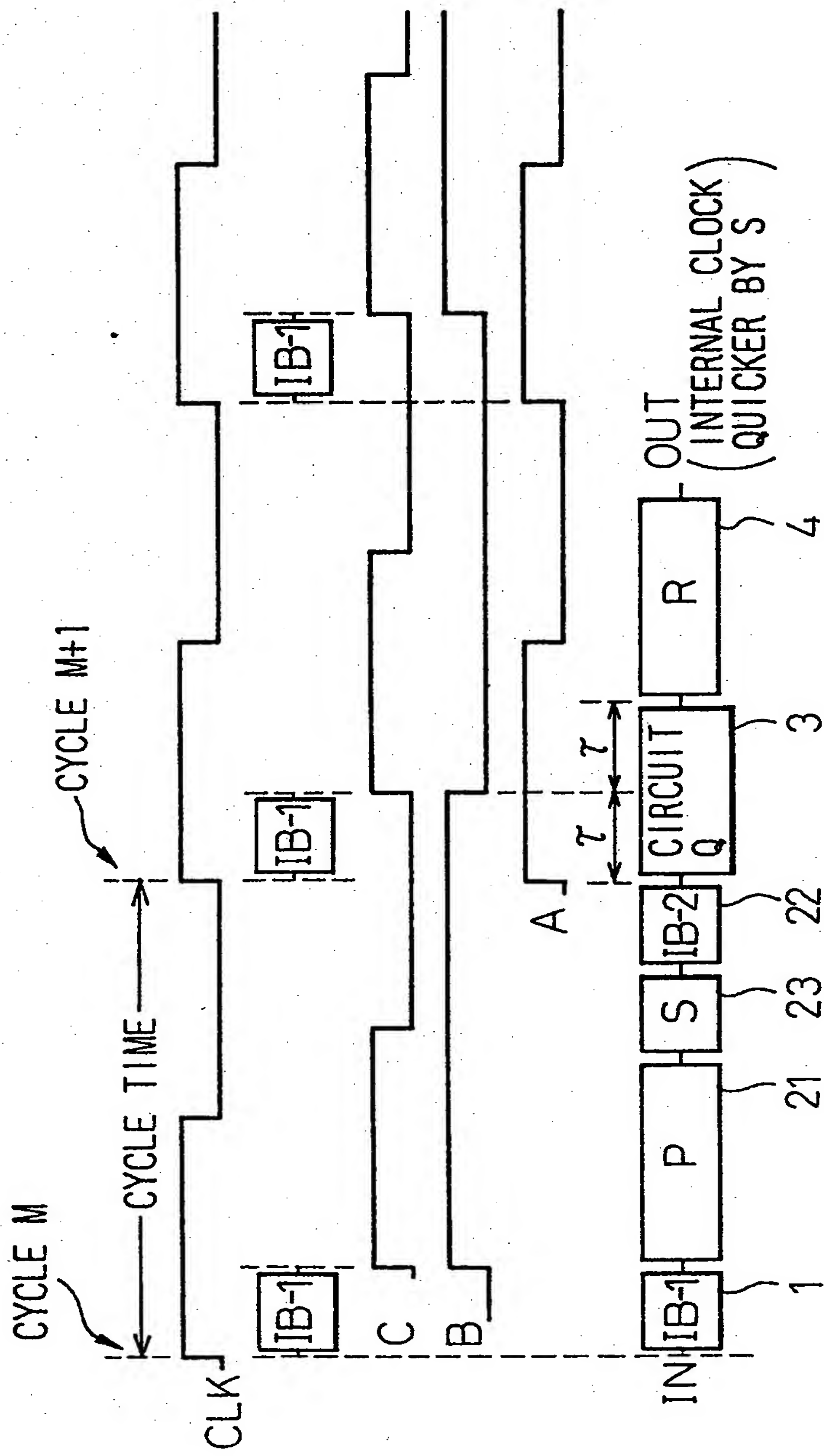


Fig. 8

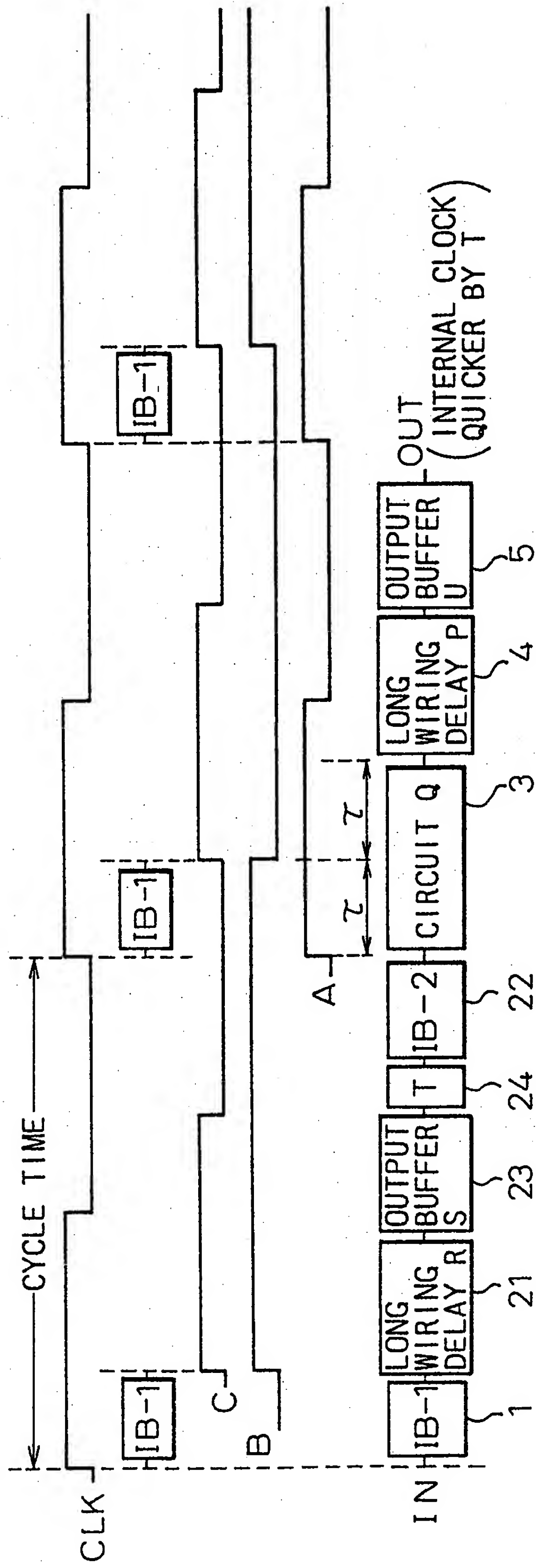


Fig. 9

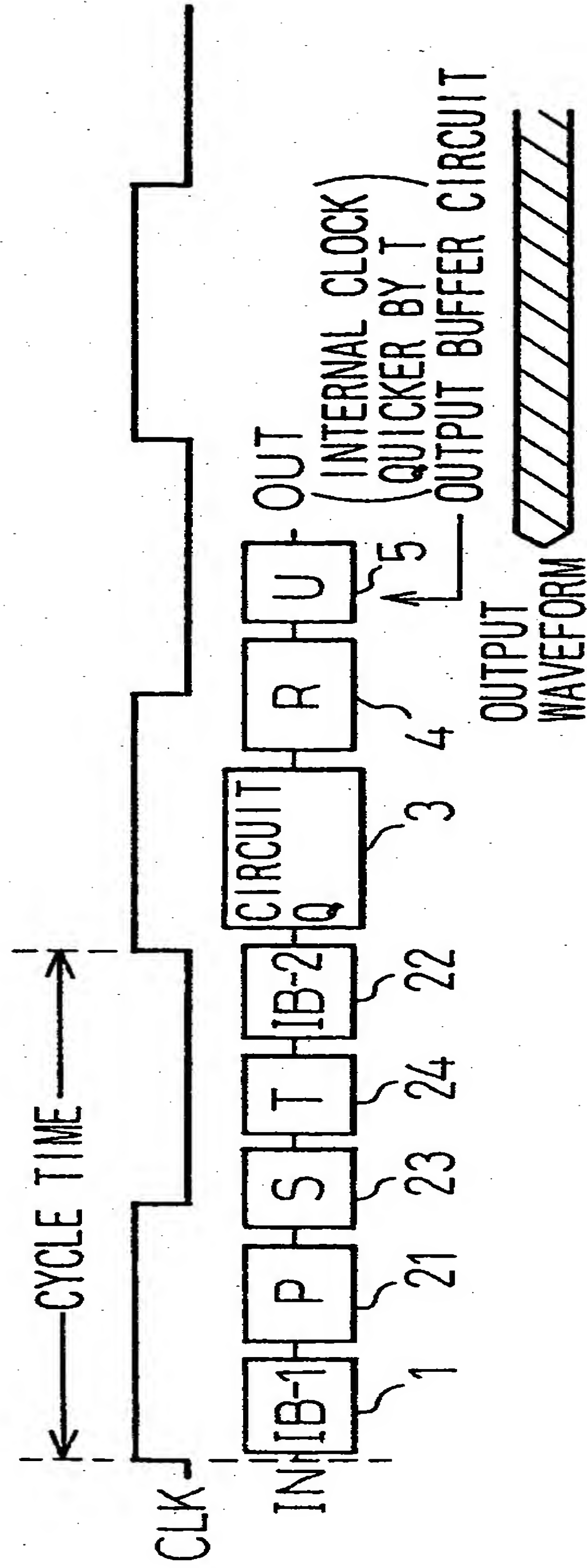
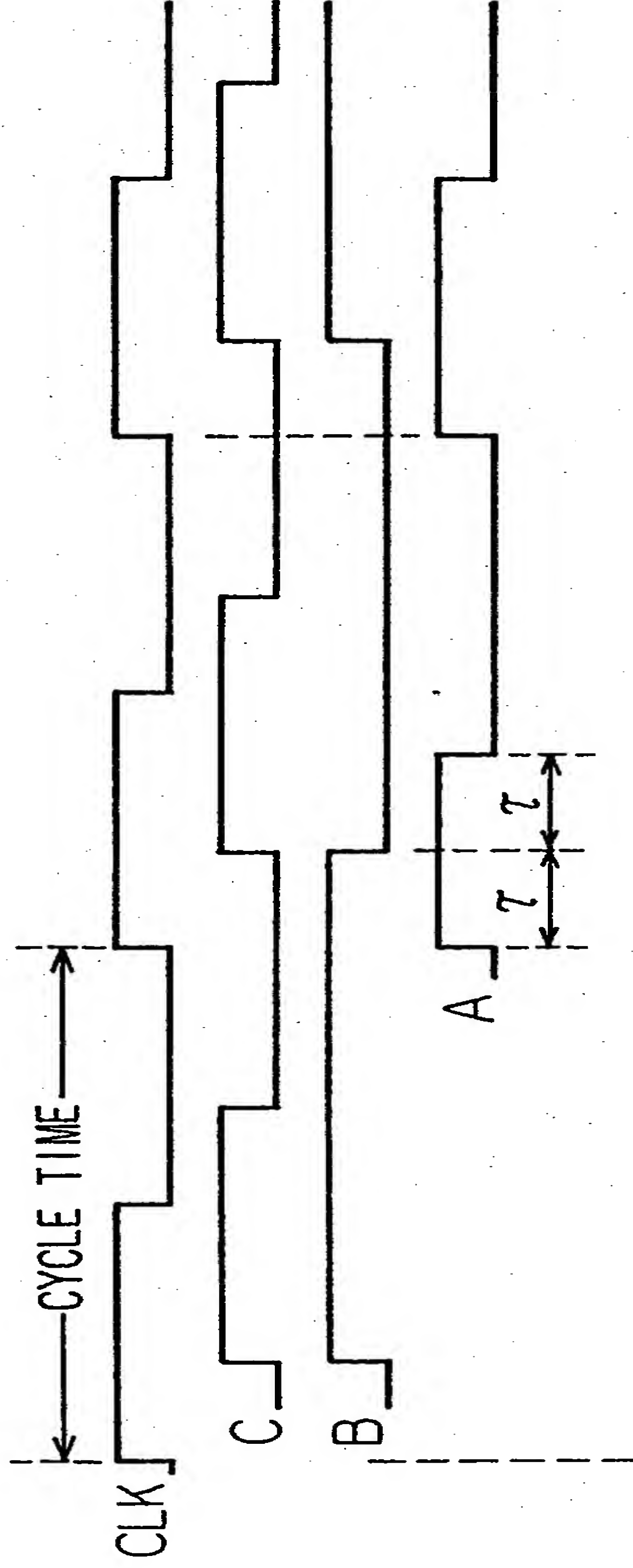


Fig.10



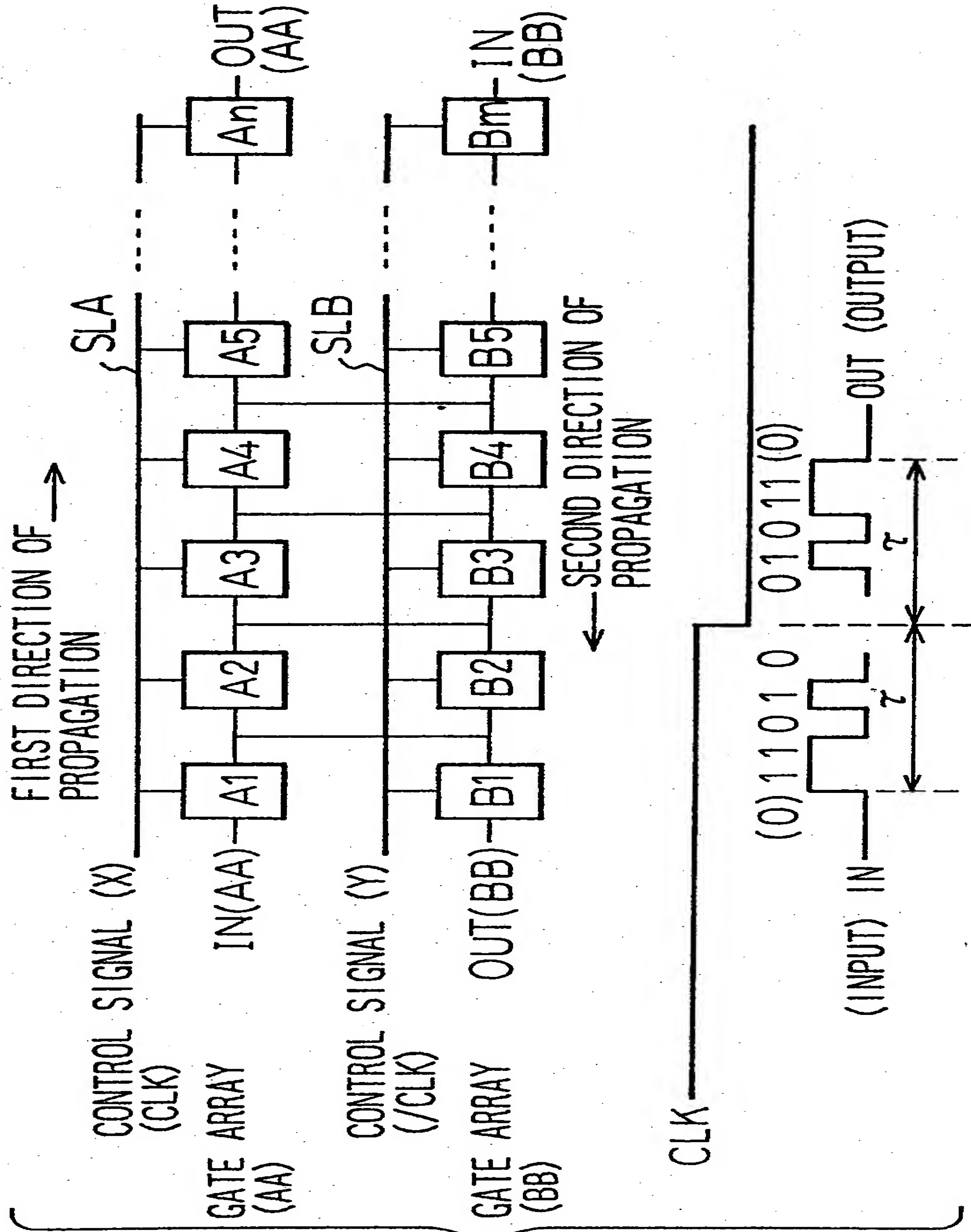
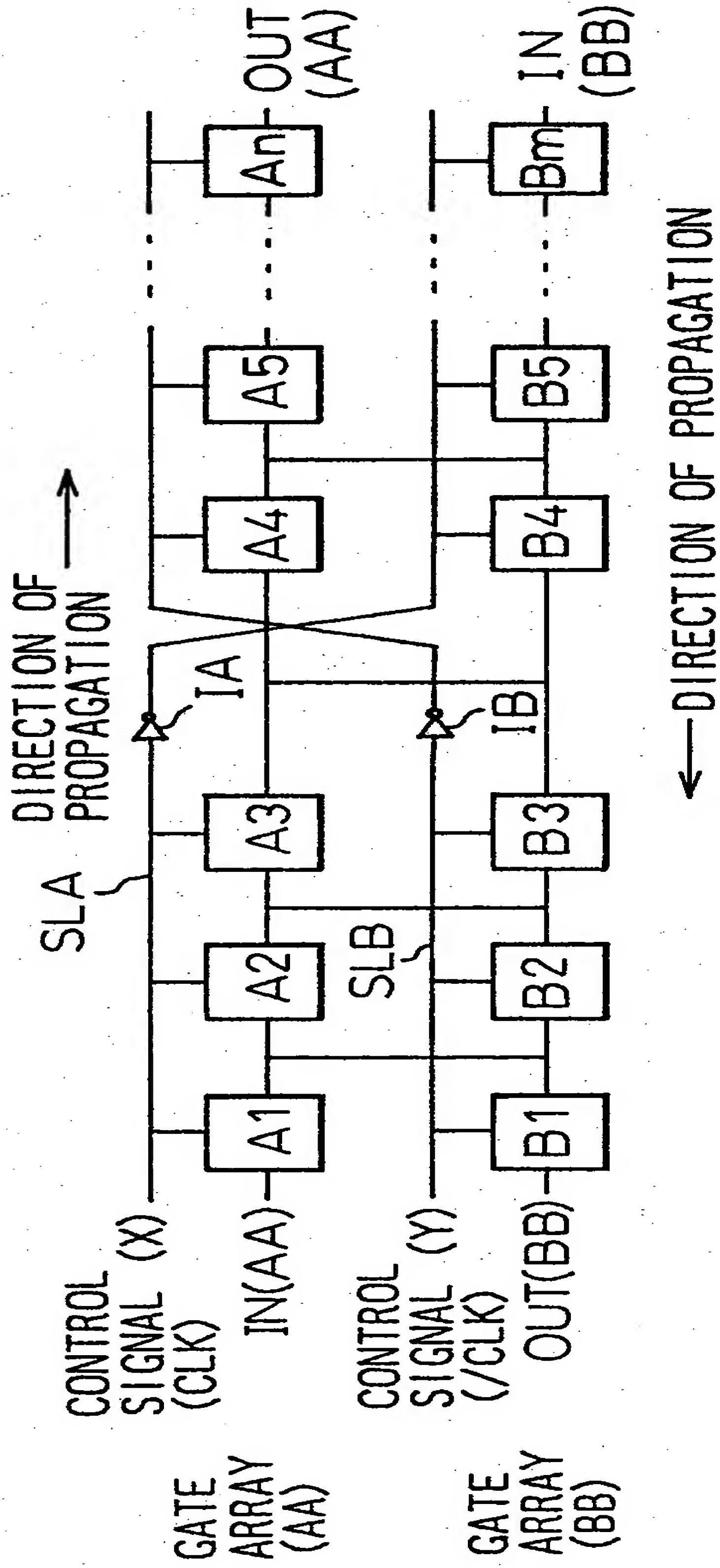


Fig.11

Fig.12



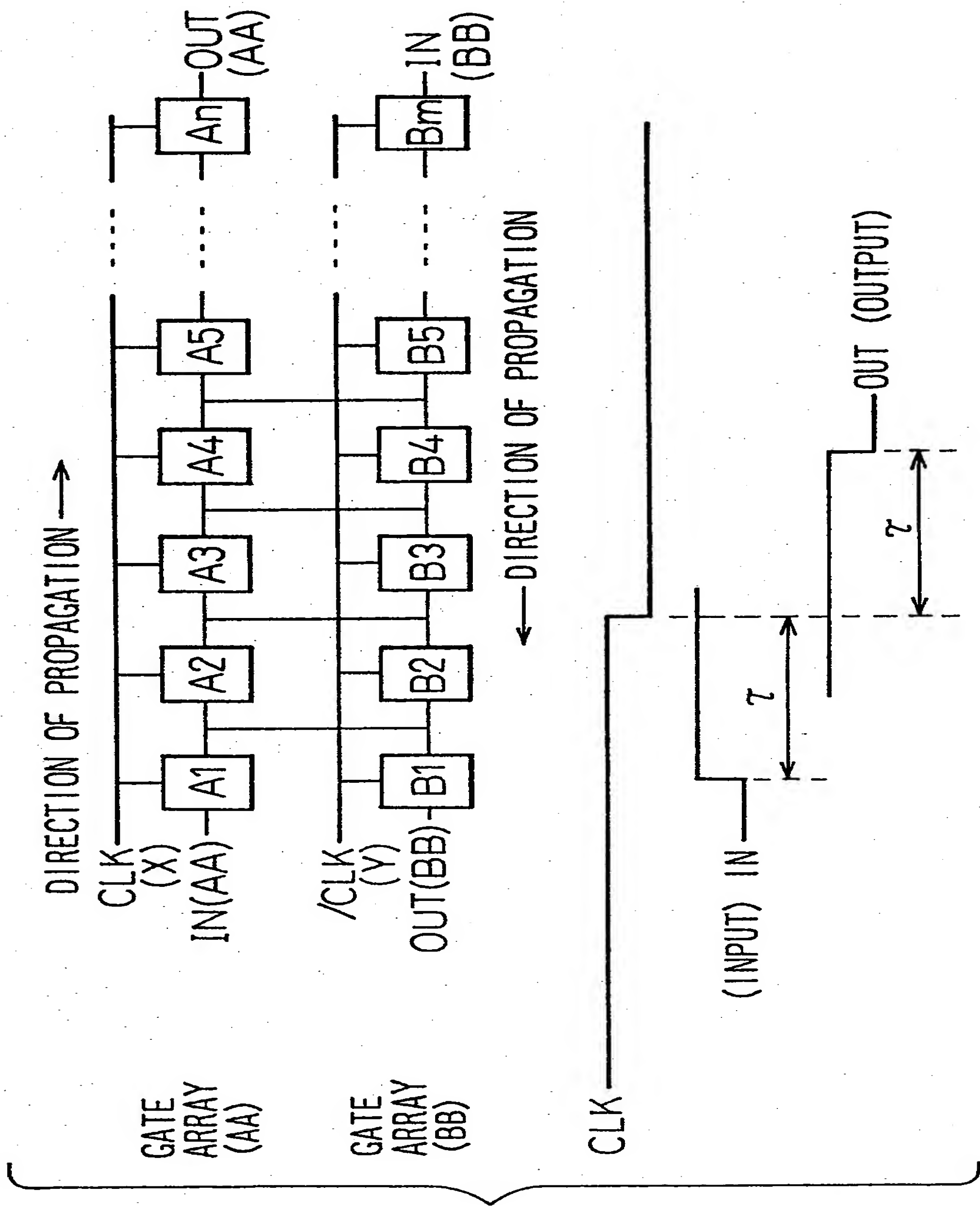


Fig.13

Fig.14

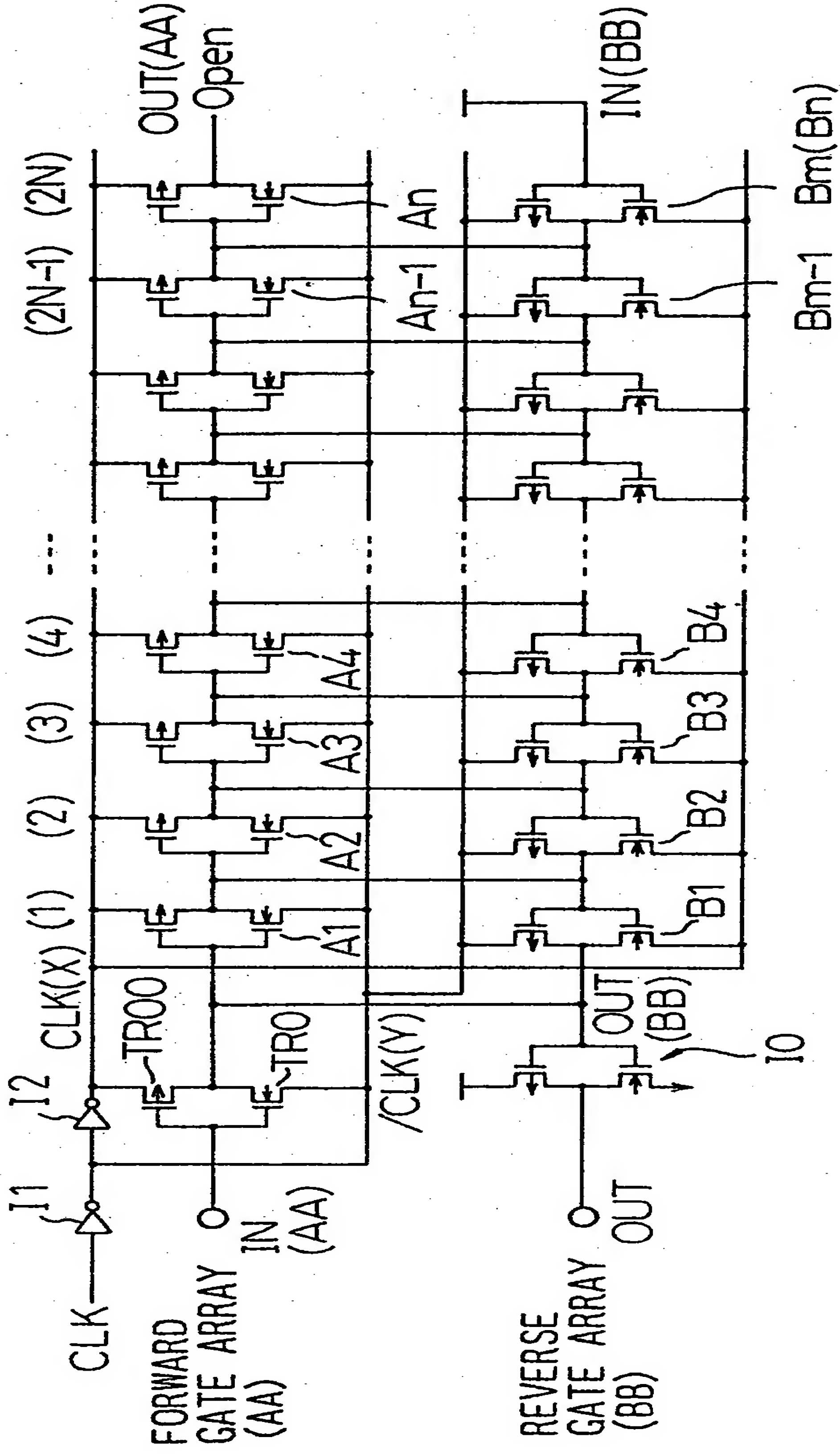


Fig.15

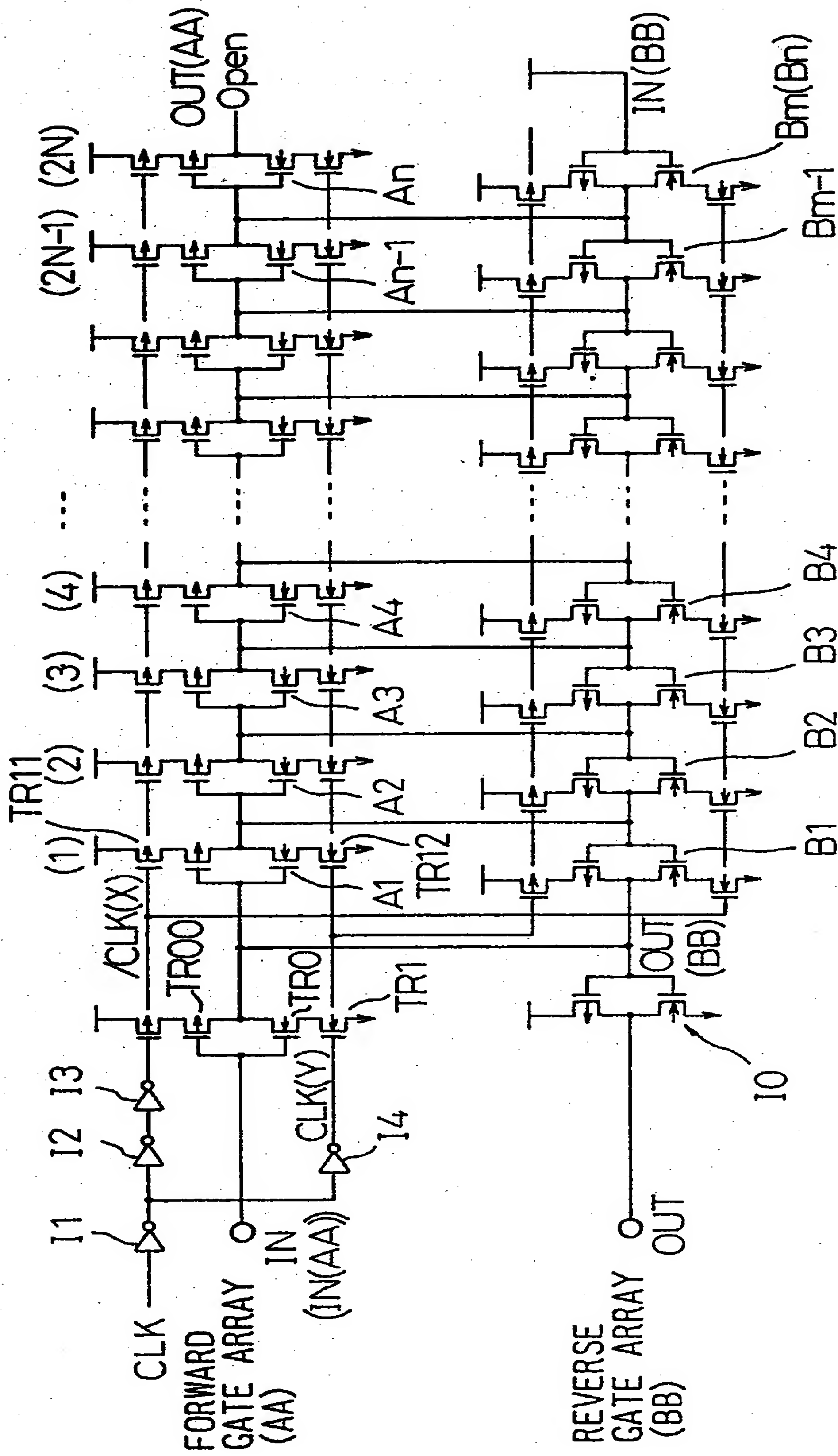


Fig. 16

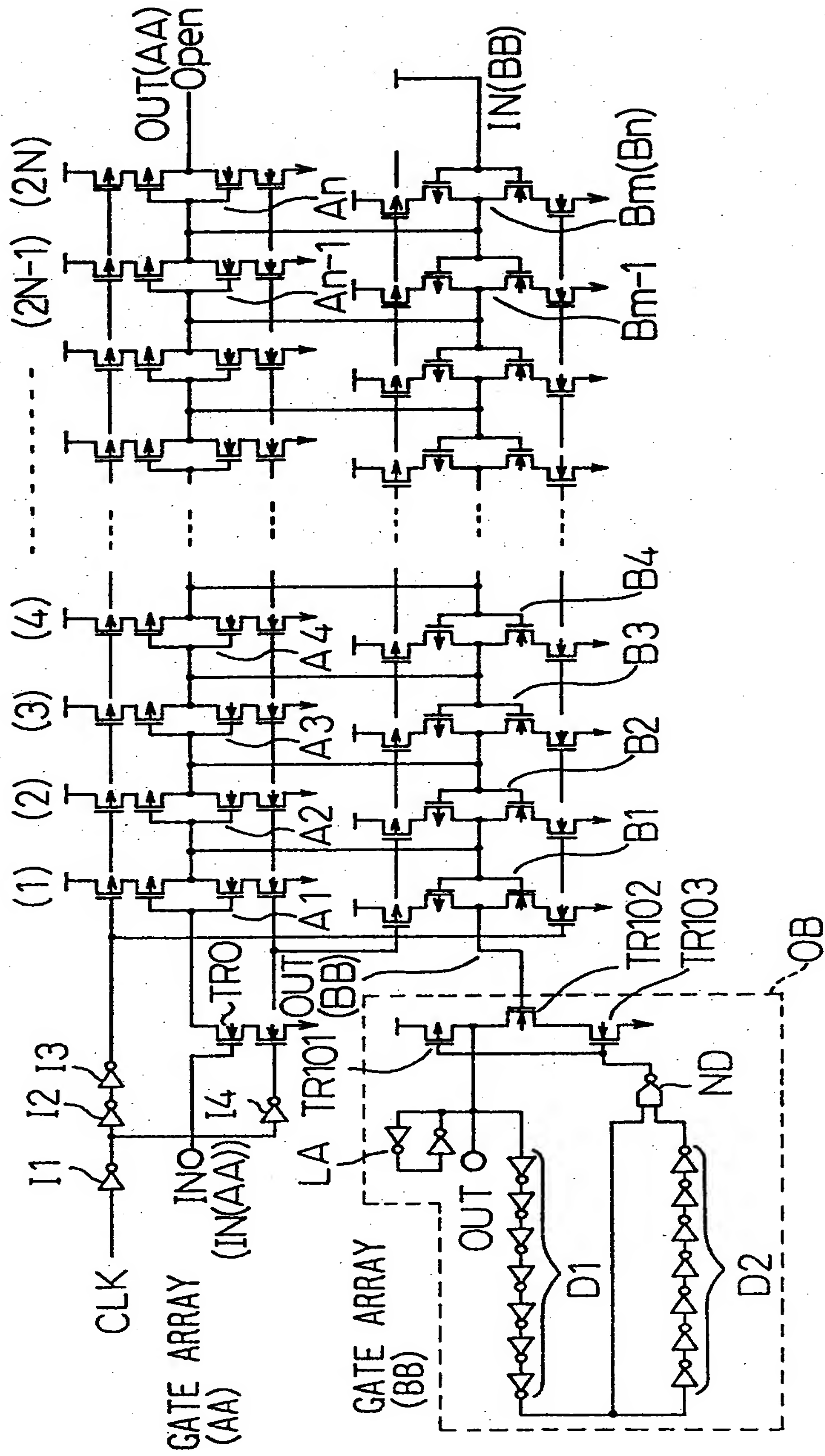


Fig. 17

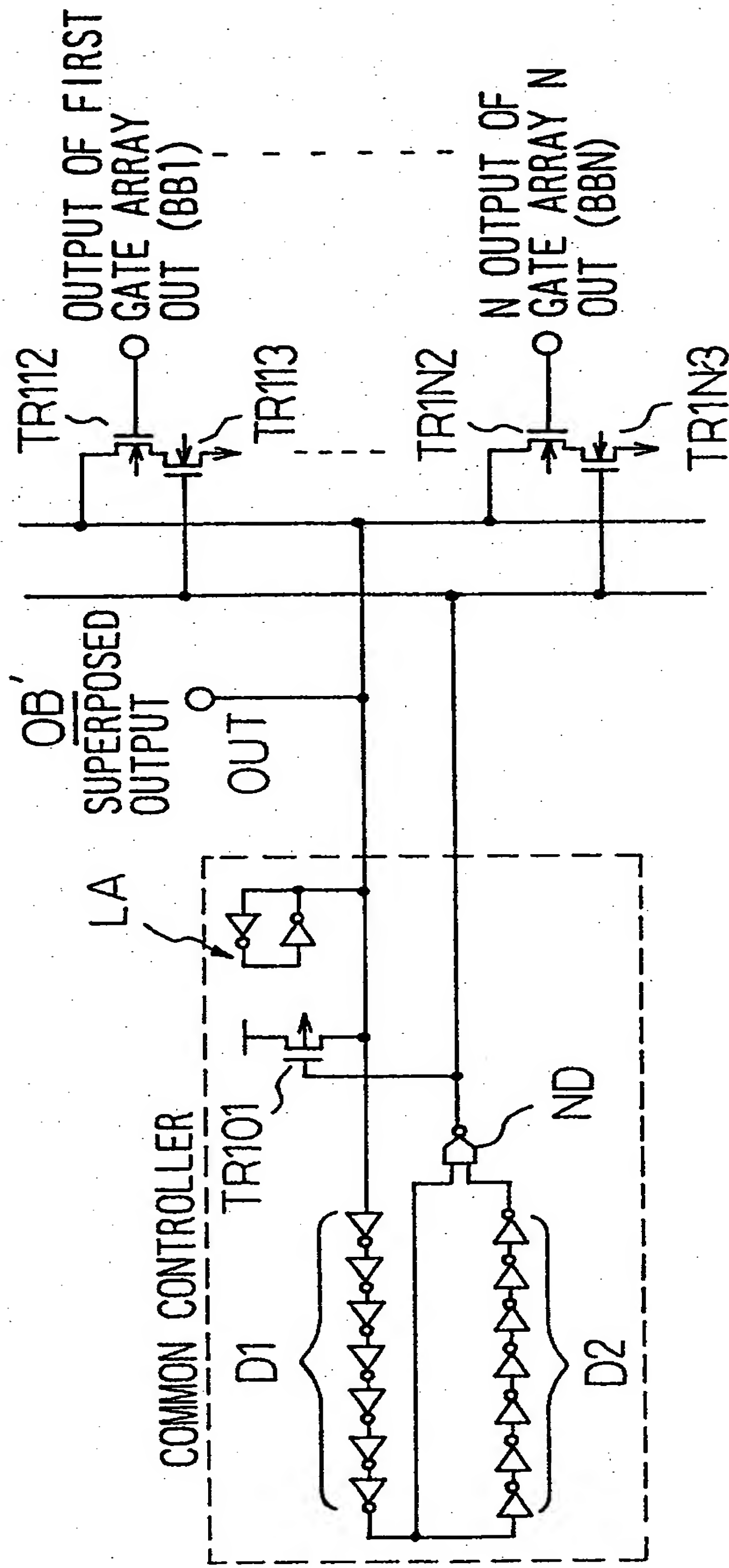


Fig.18

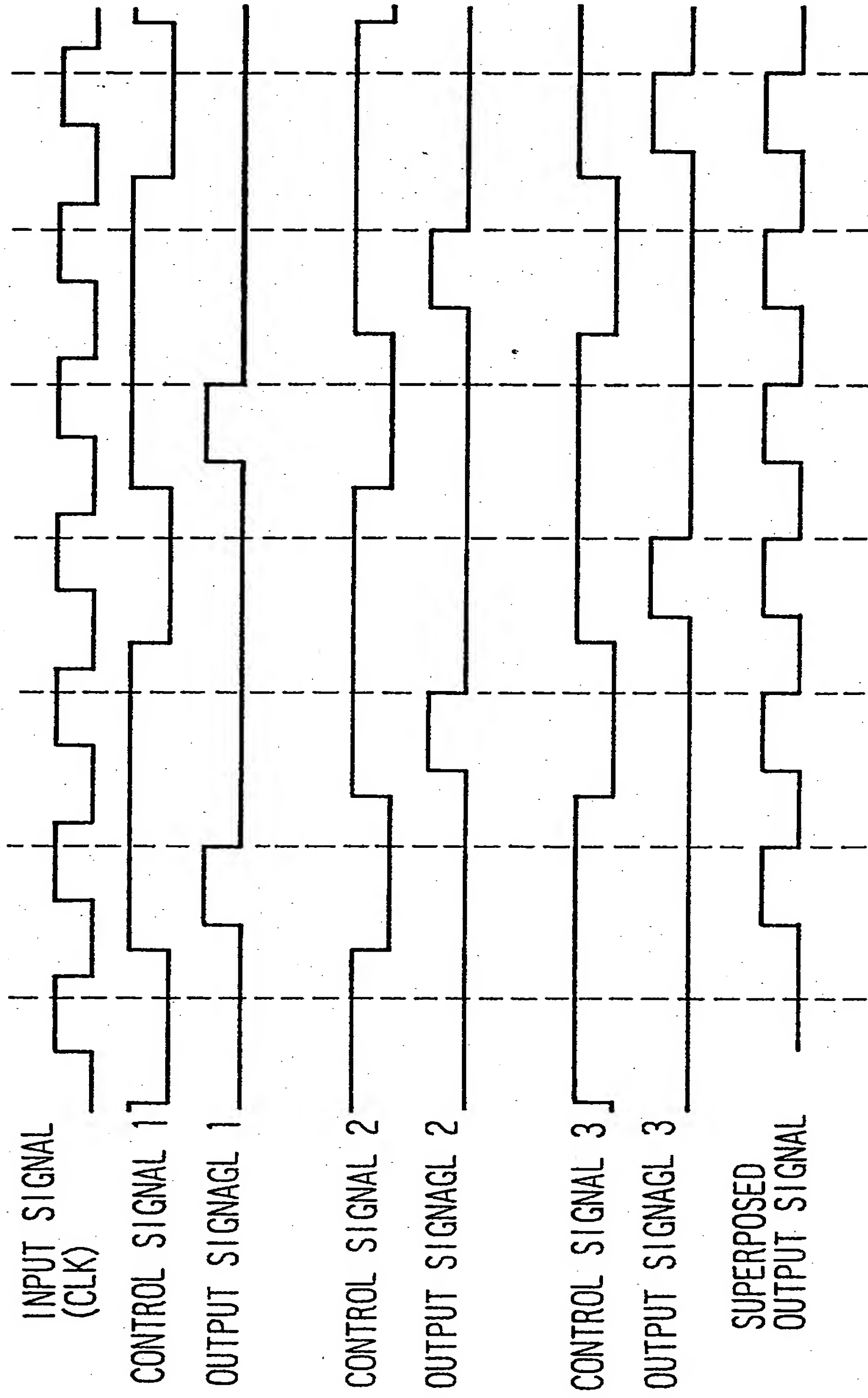


Fig. 19

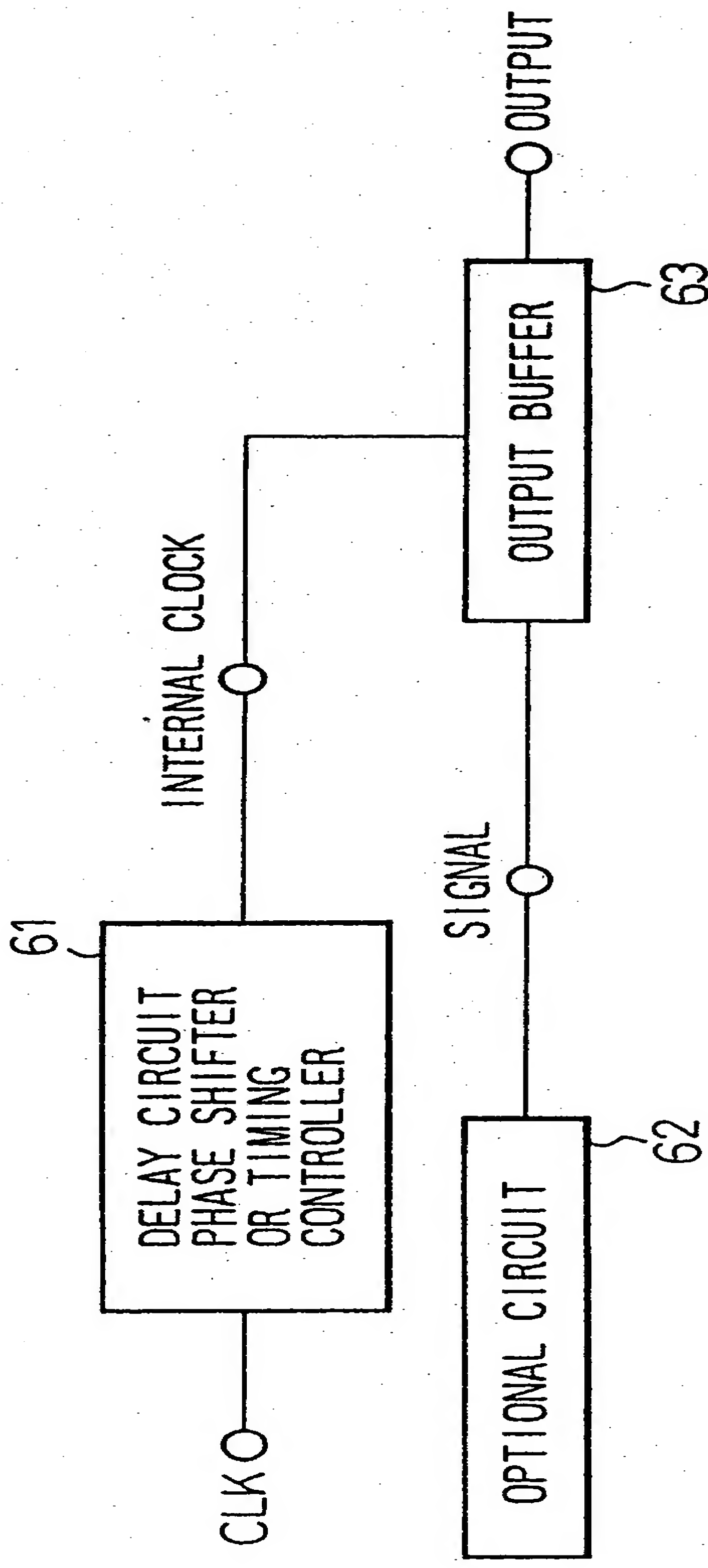


Fig. 20A

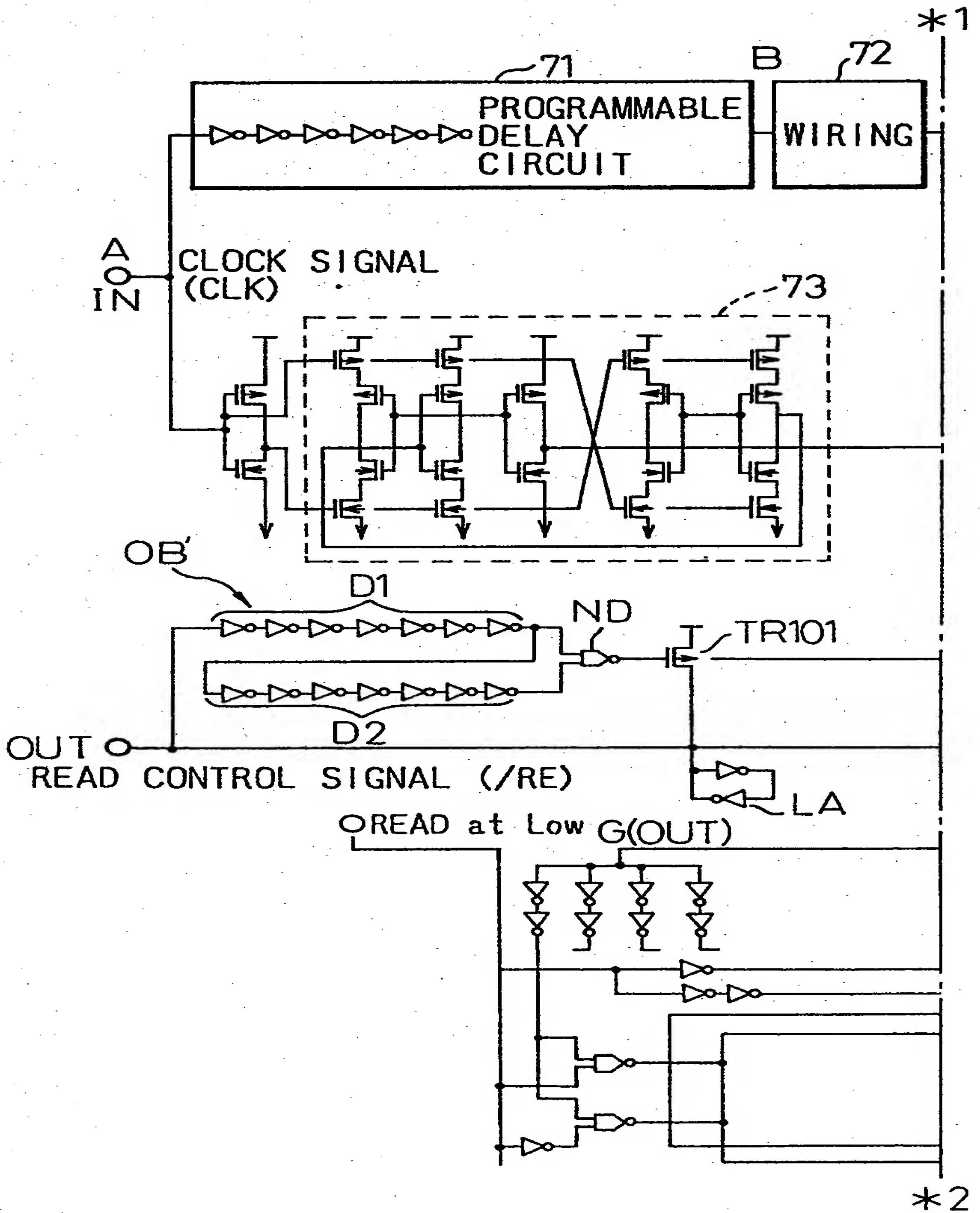


Fig. 20B

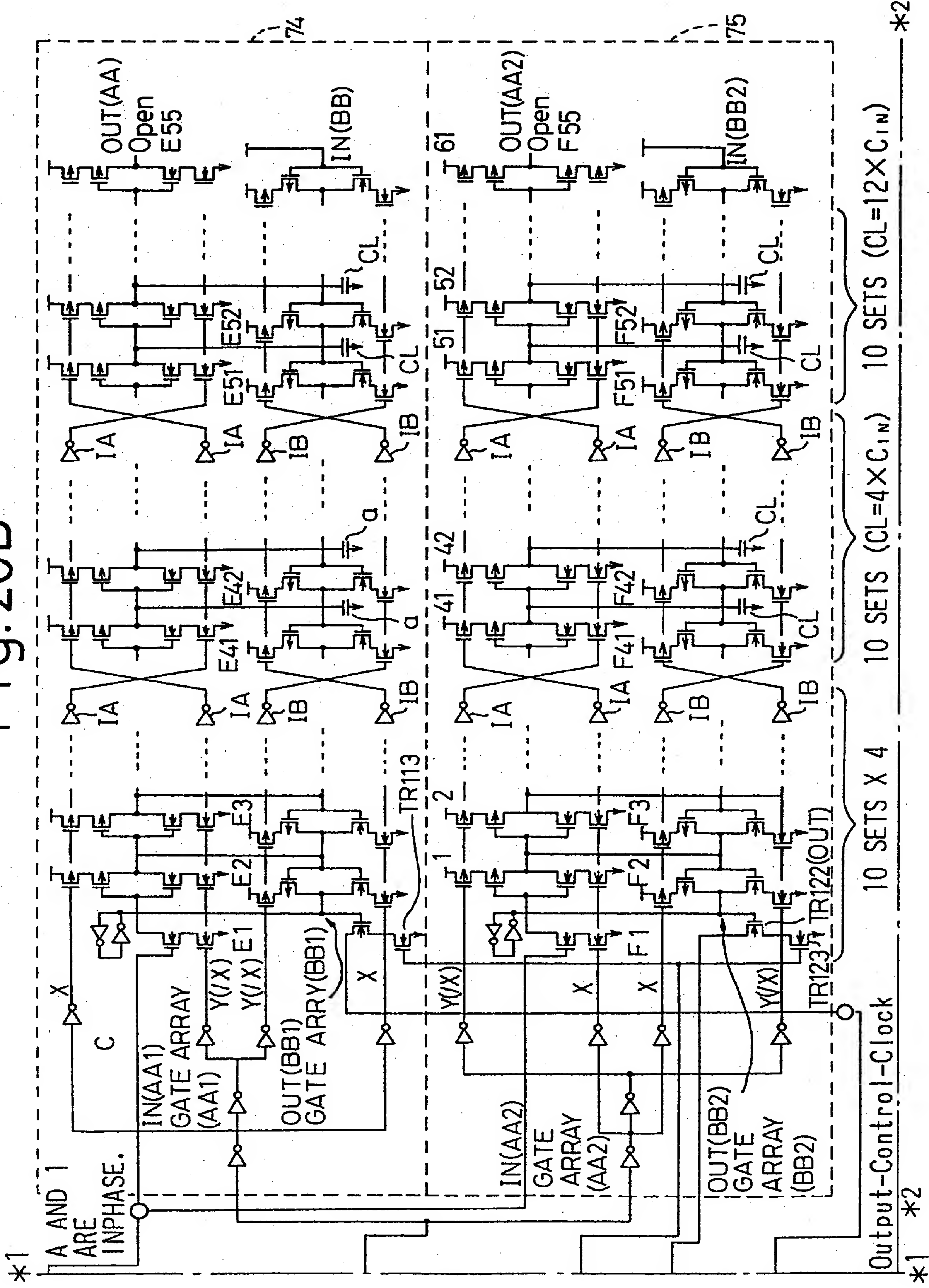


Fig. 20C

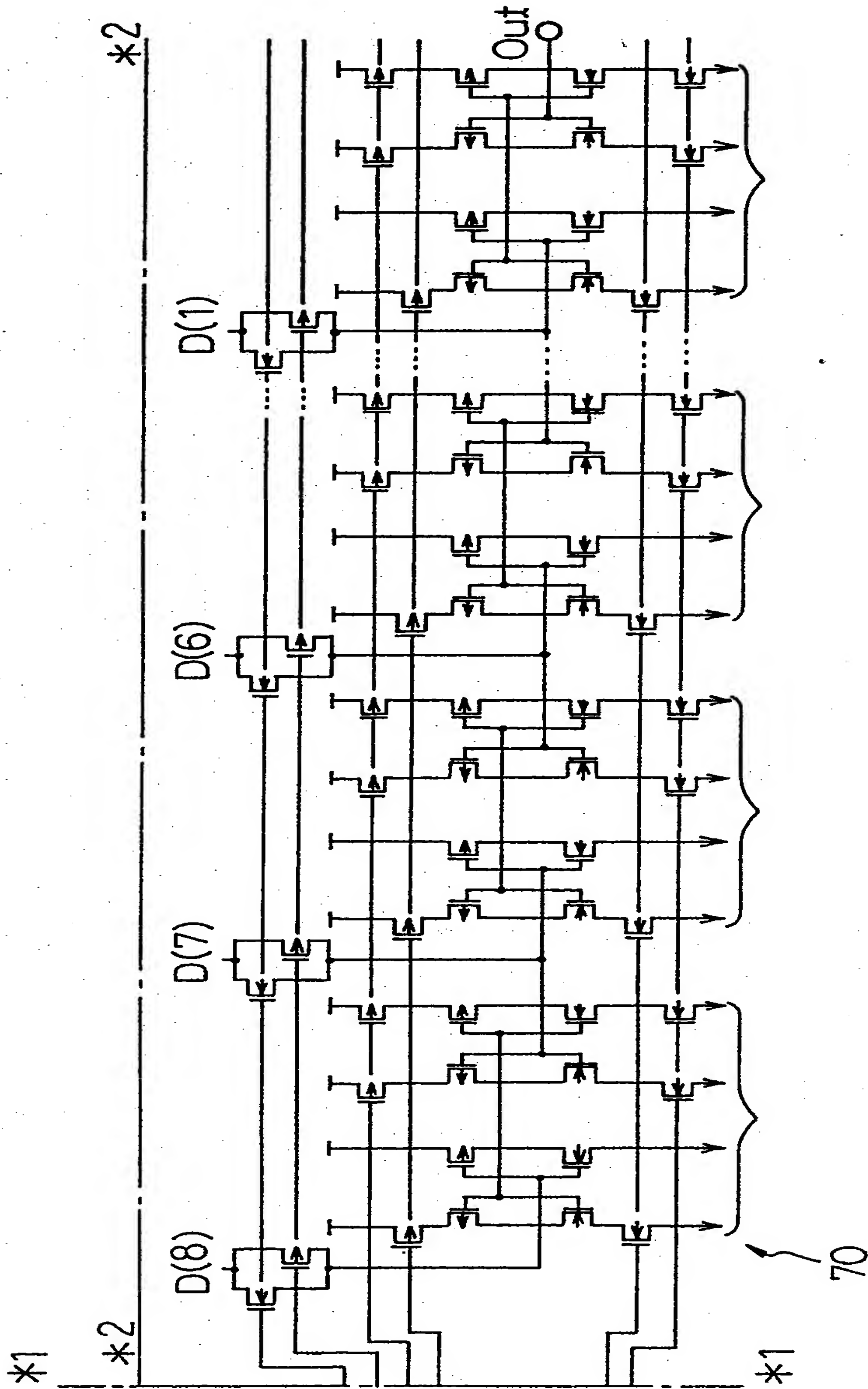


Fig. 21A

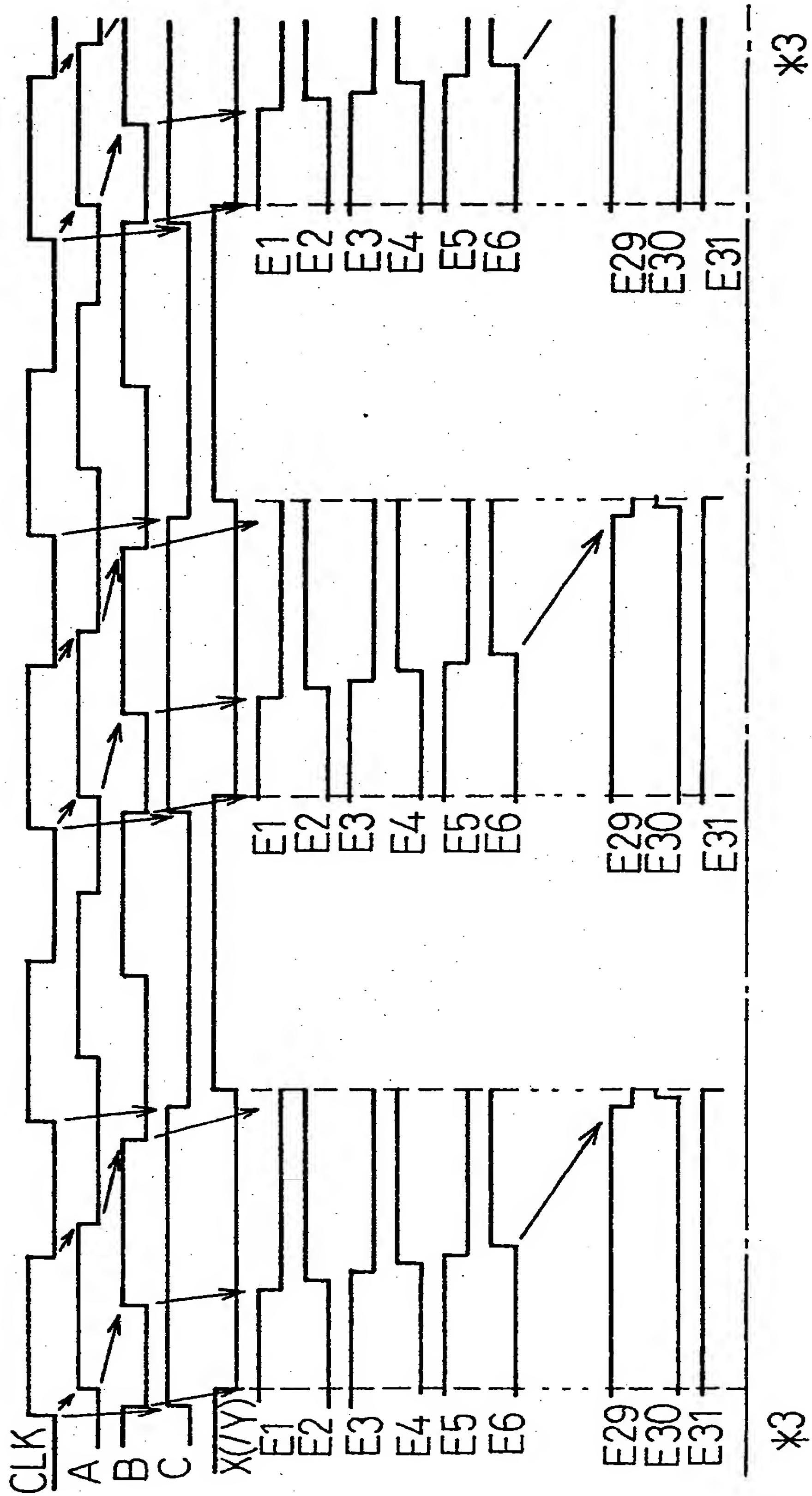


Fig. 21B

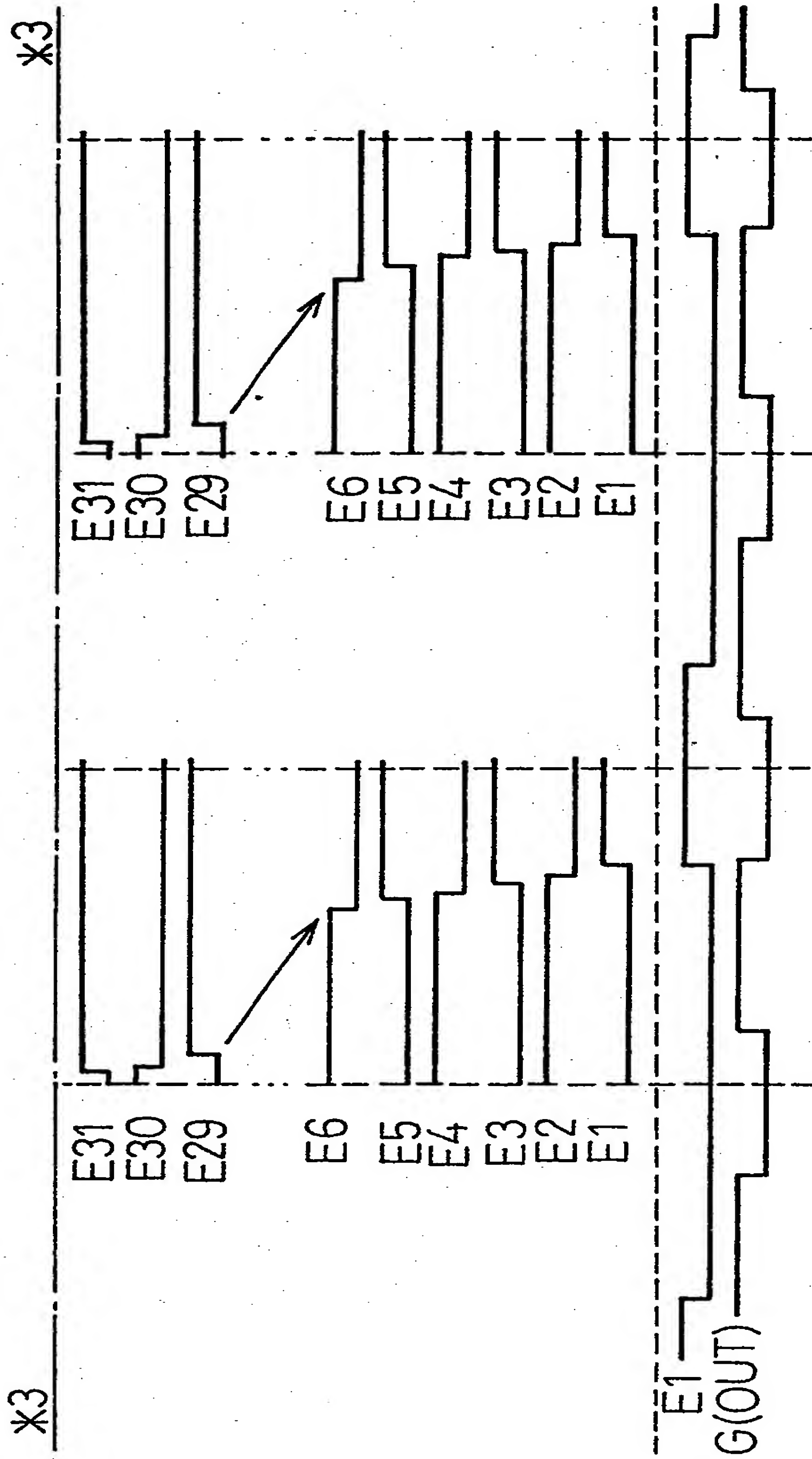


Fig. 22

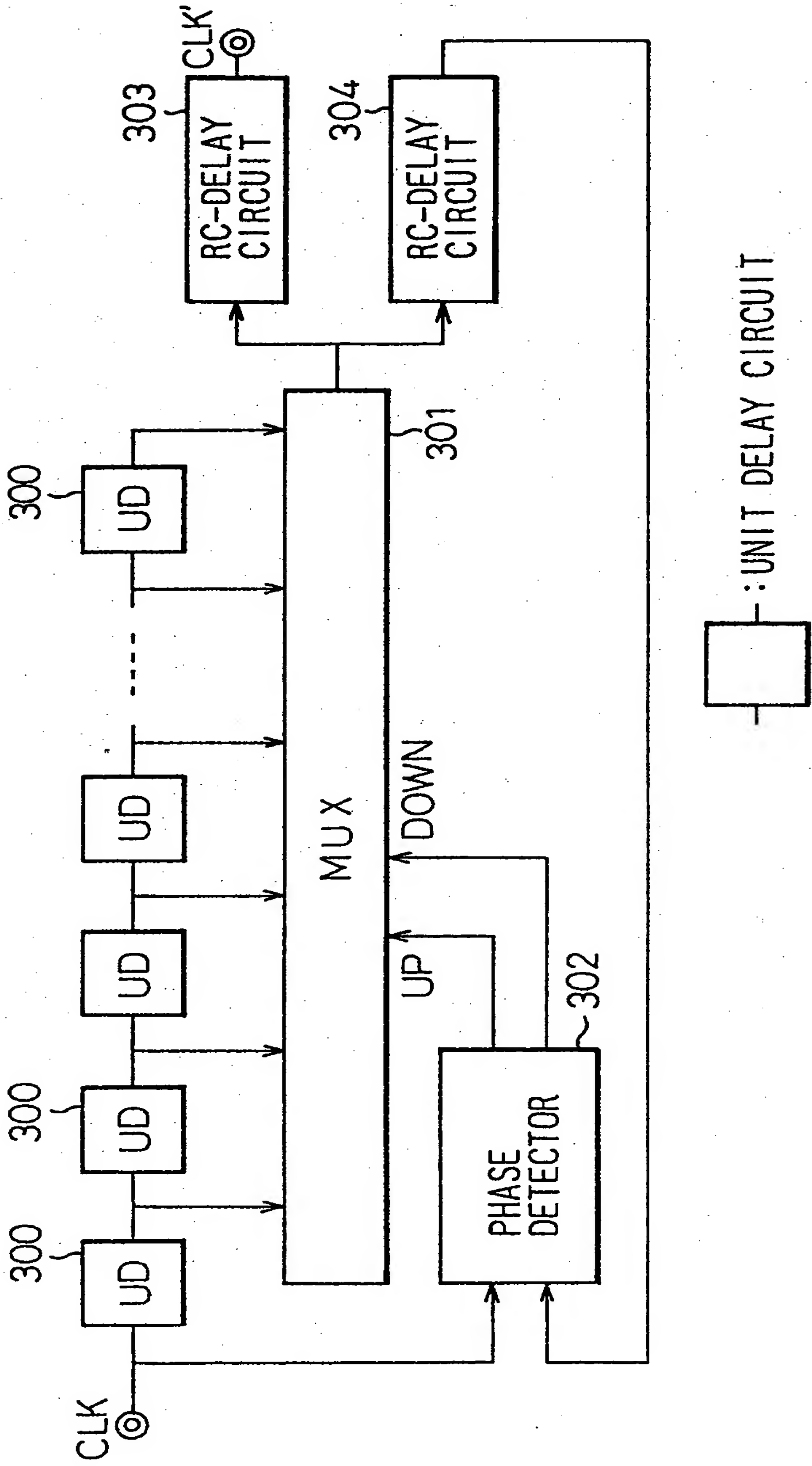


Fig. 23

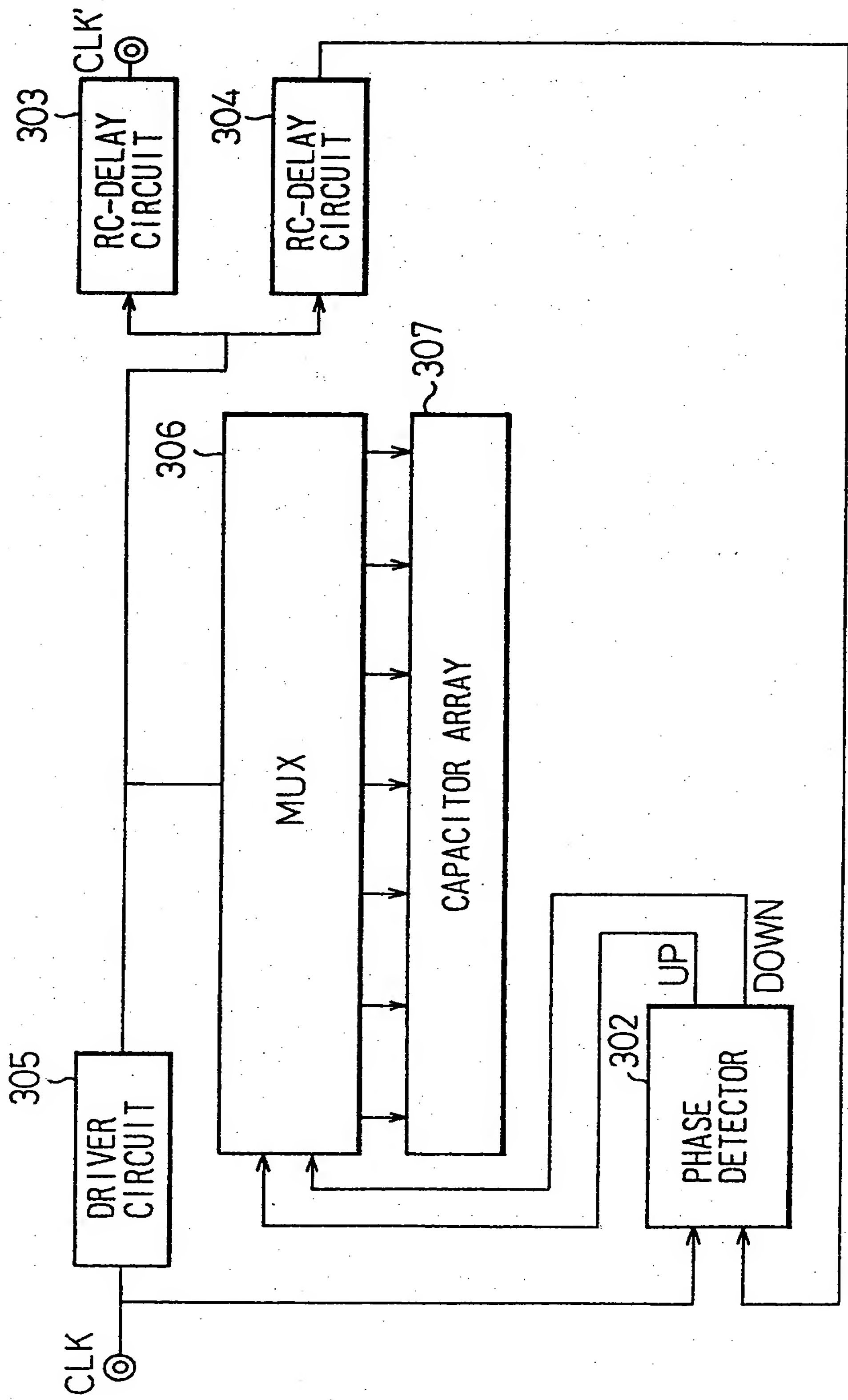


Fig. 24

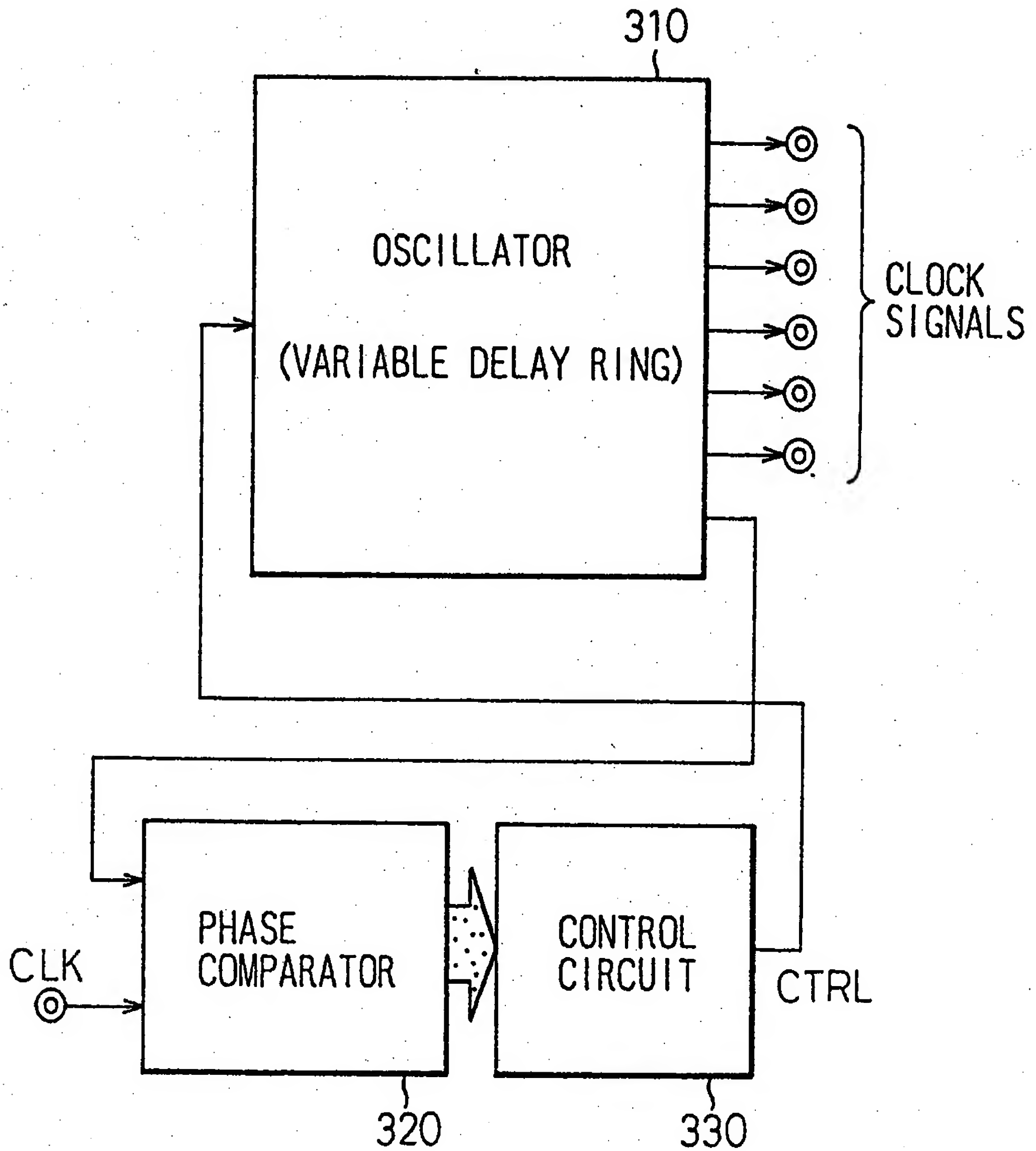


Fig. 25

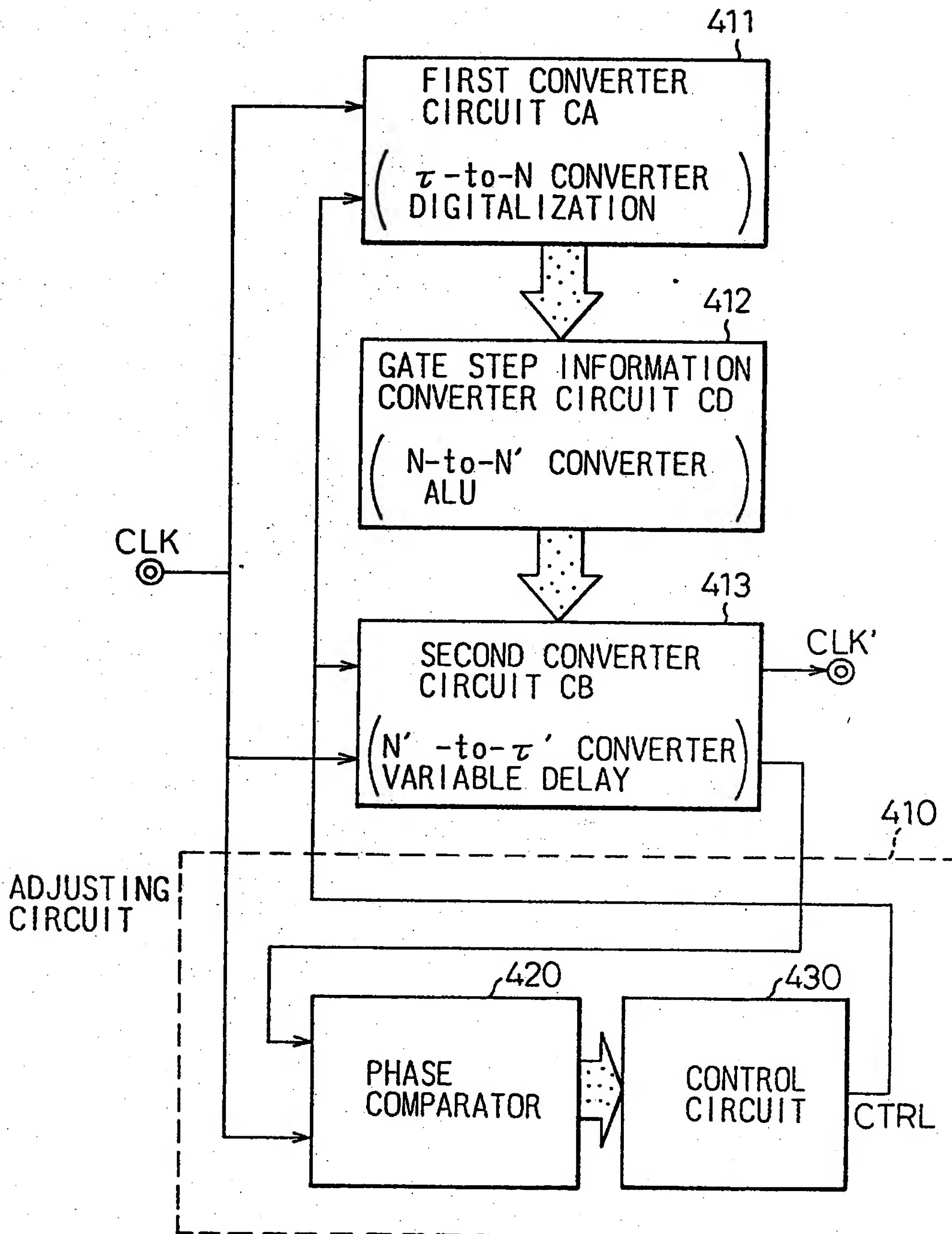


Fig. 26A

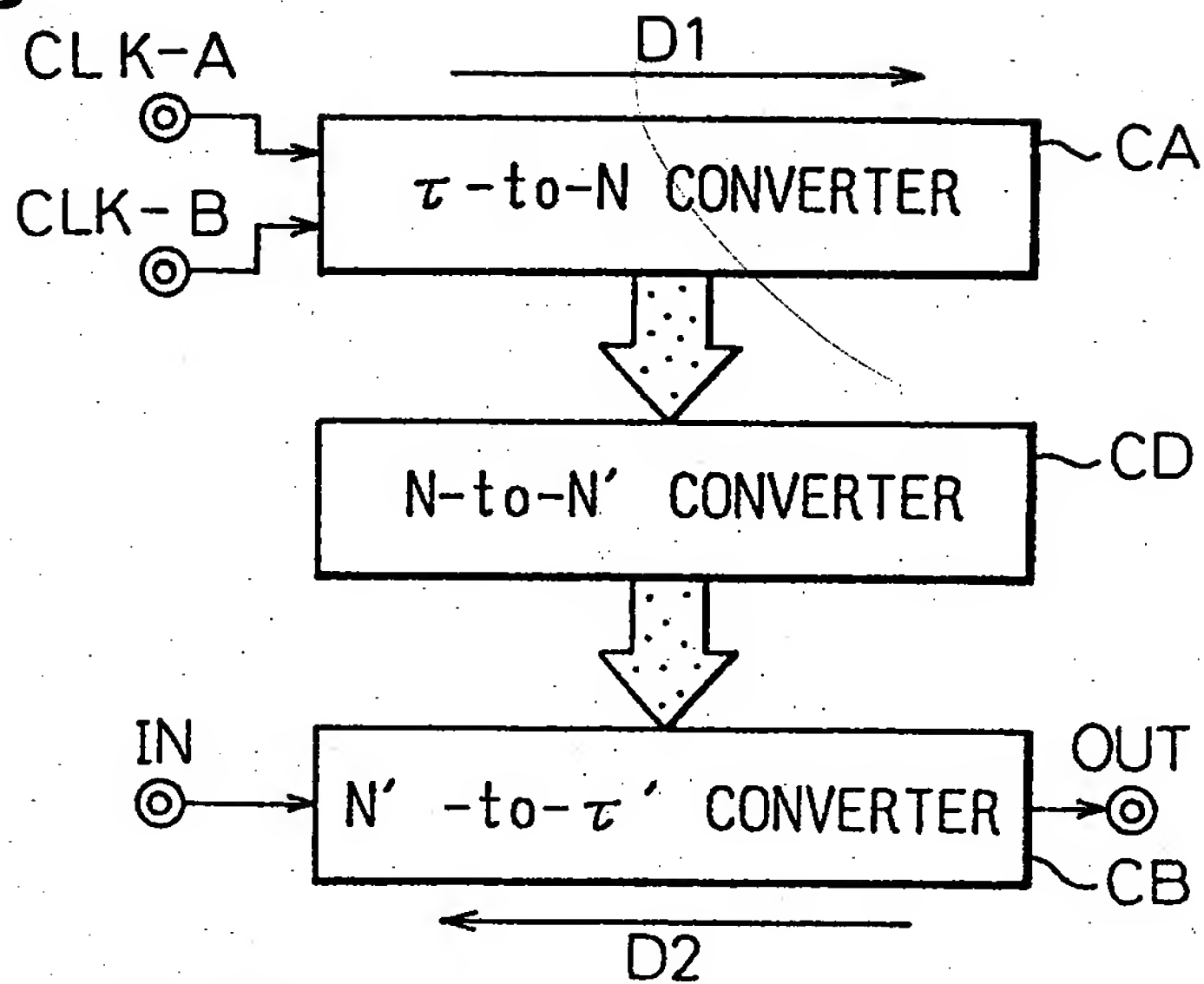


Fig. 26B

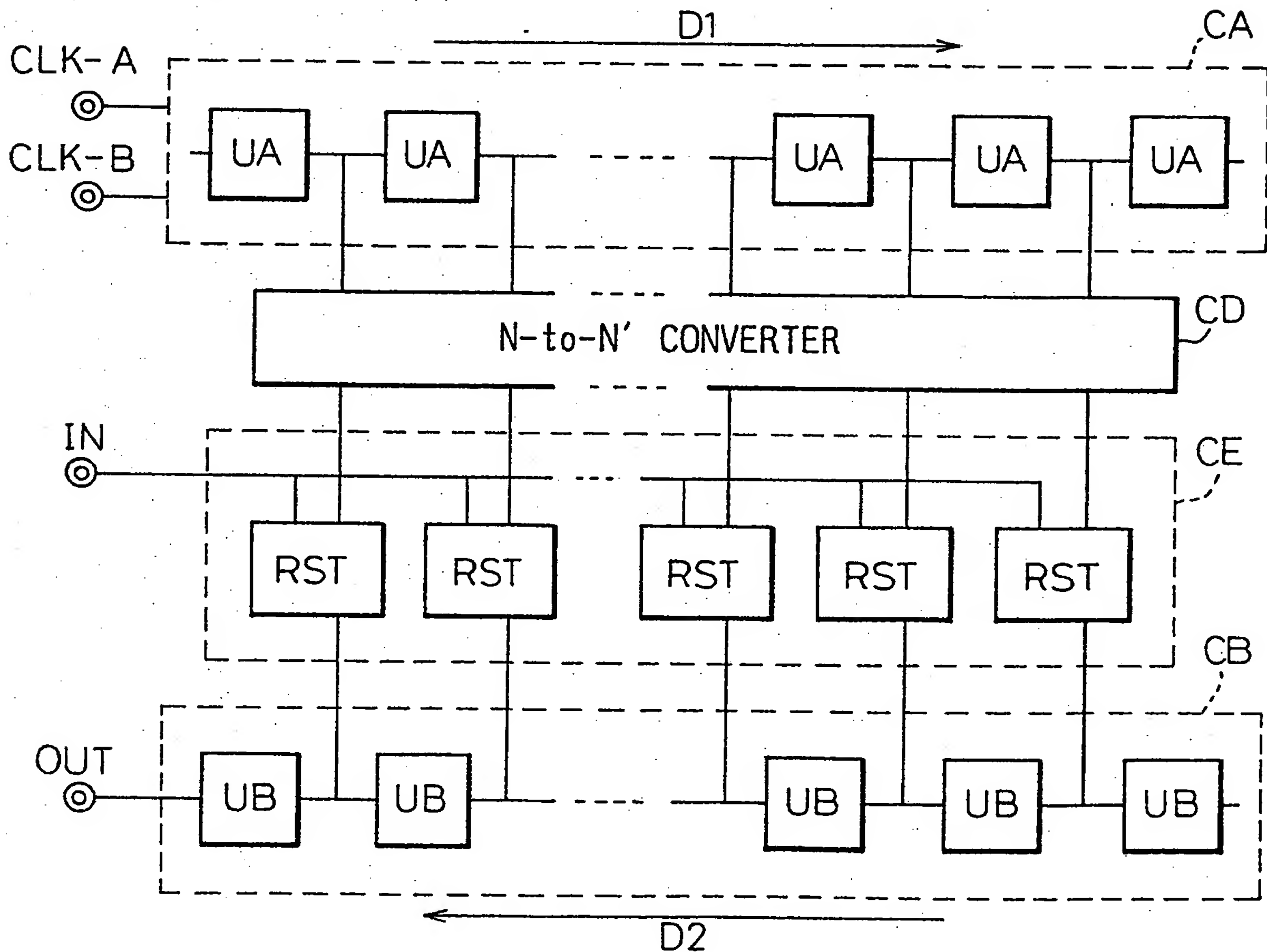


Fig. 27A

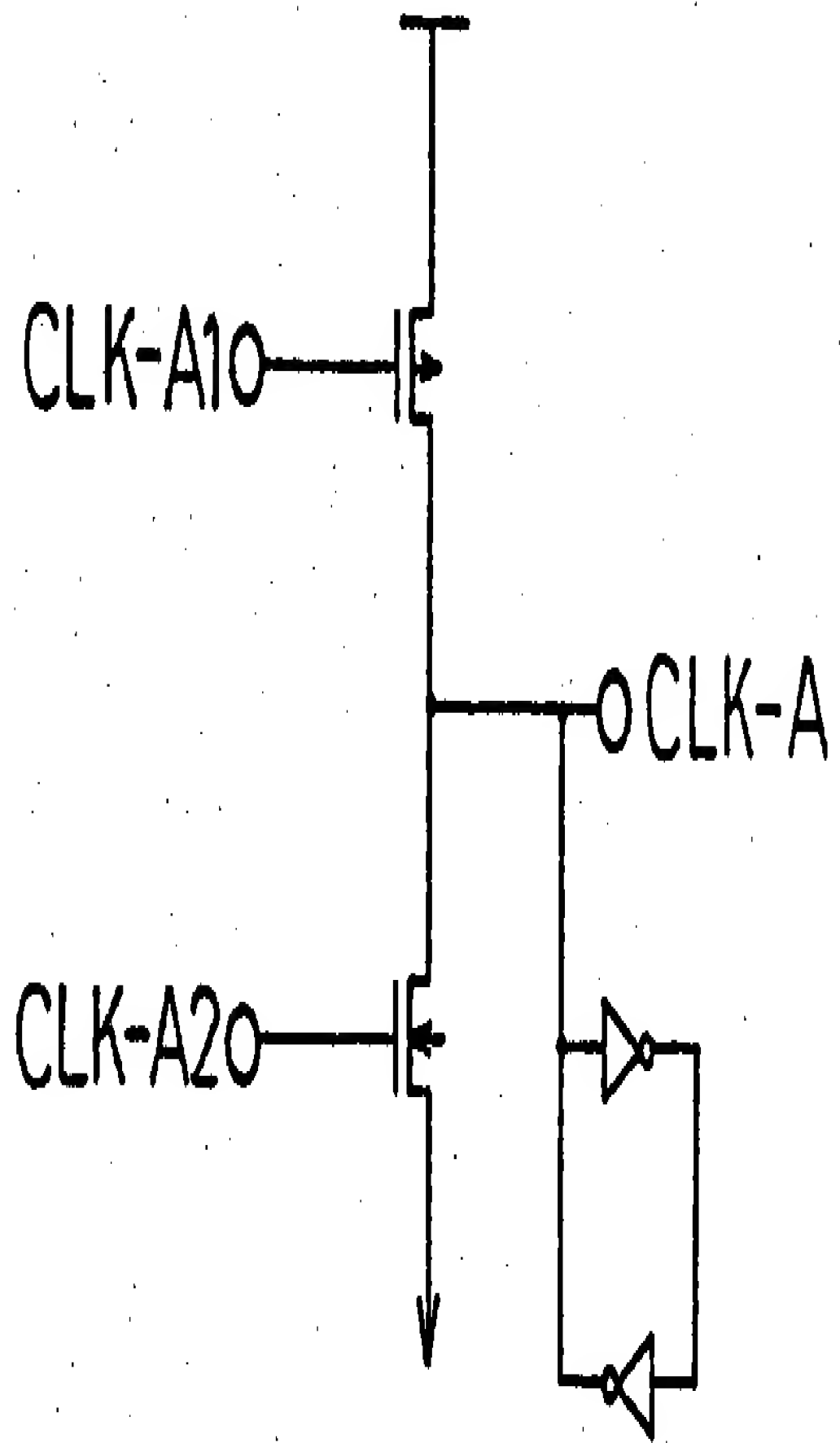
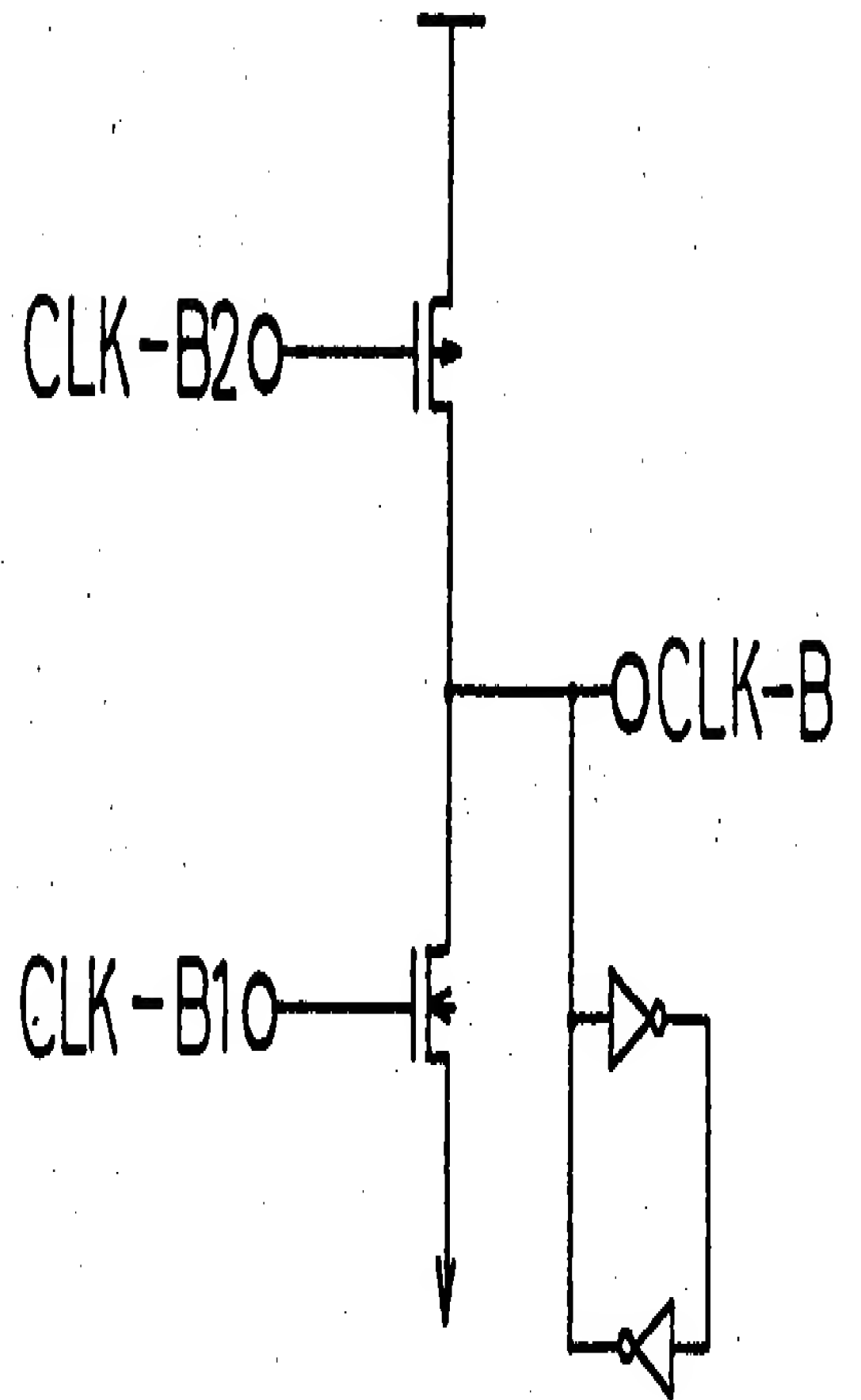


Fig. 27B



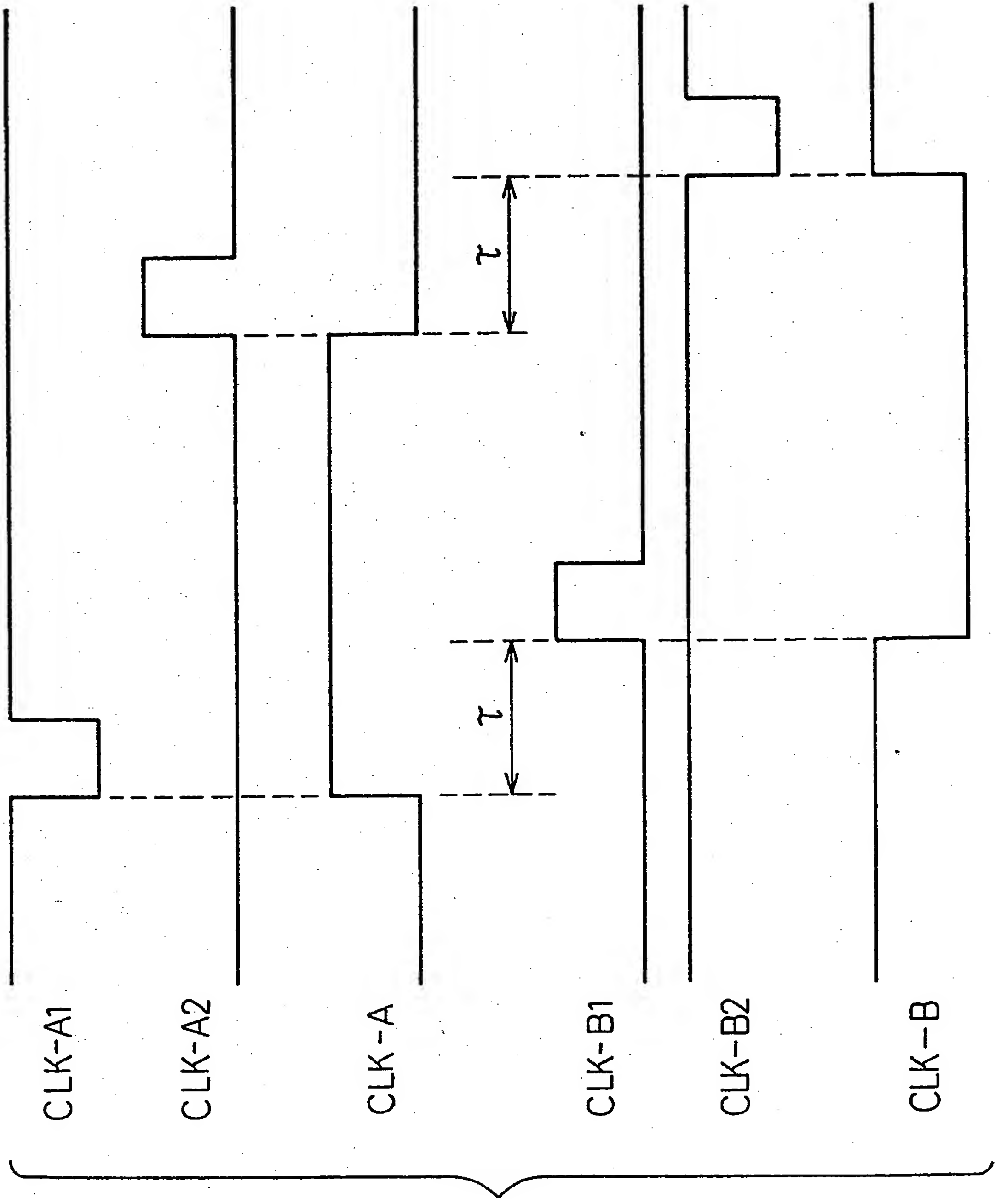


Fig. 27C

Fig. 28

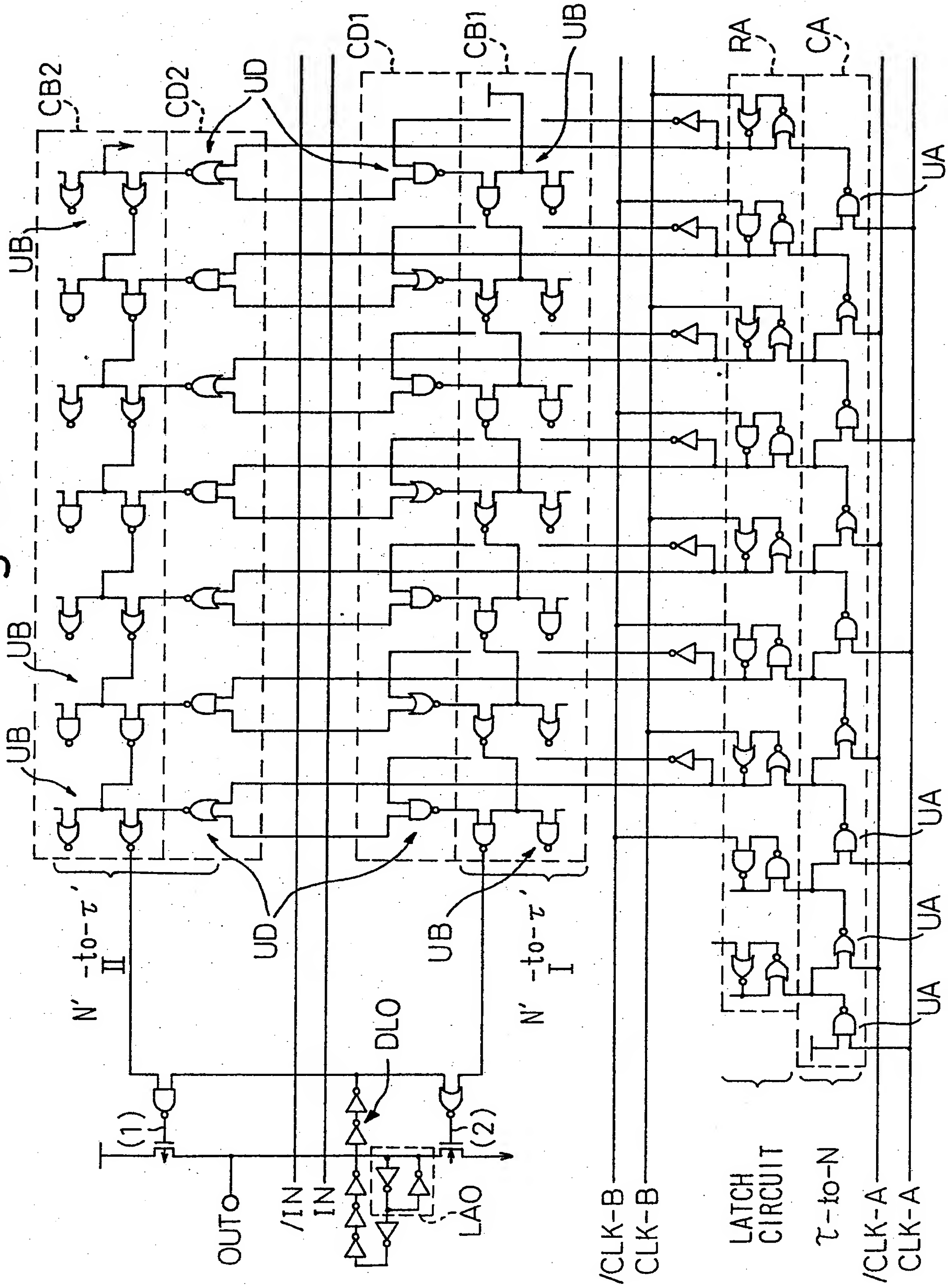


Fig. 29

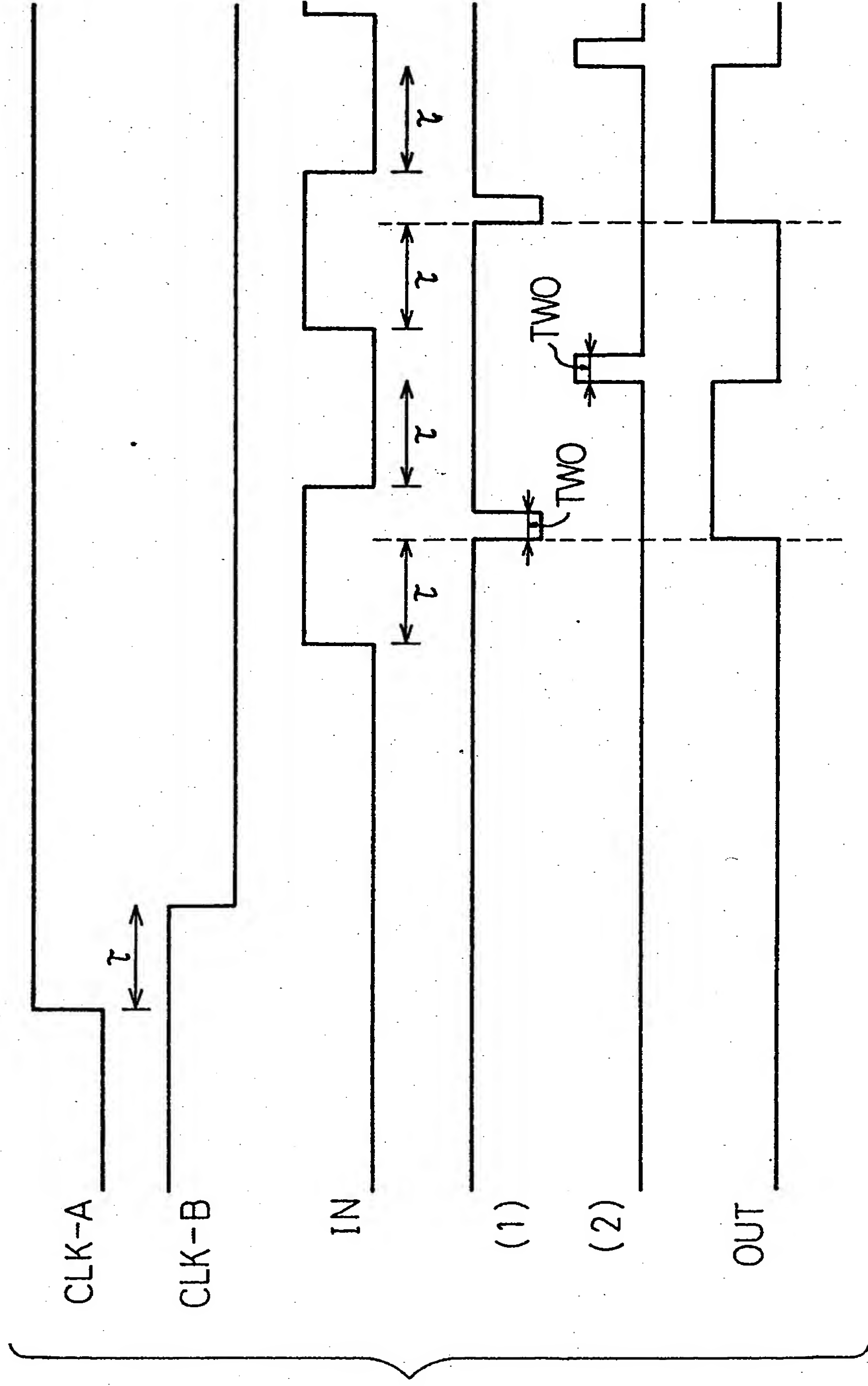


Fig. 30A

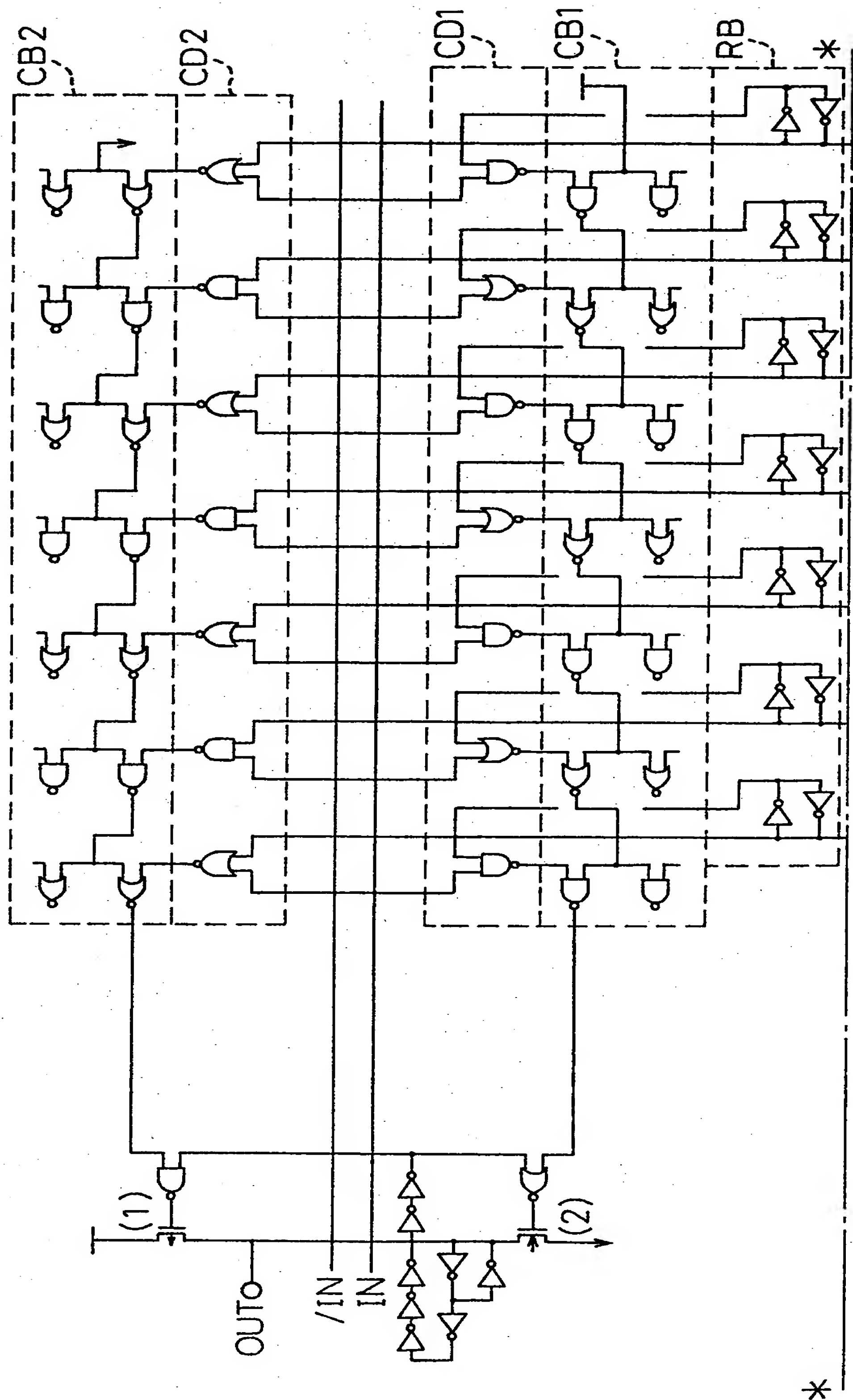
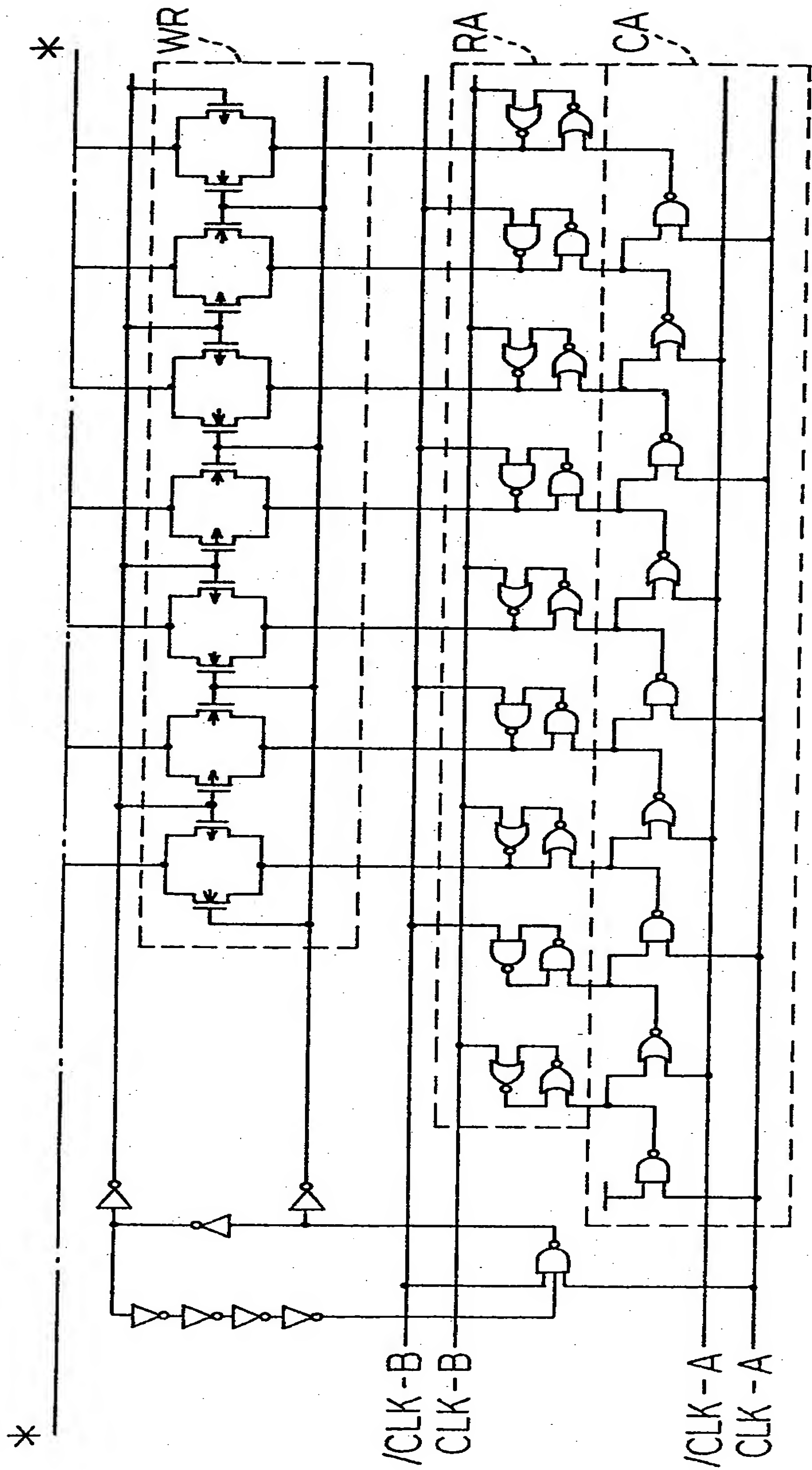


Fig. 30B



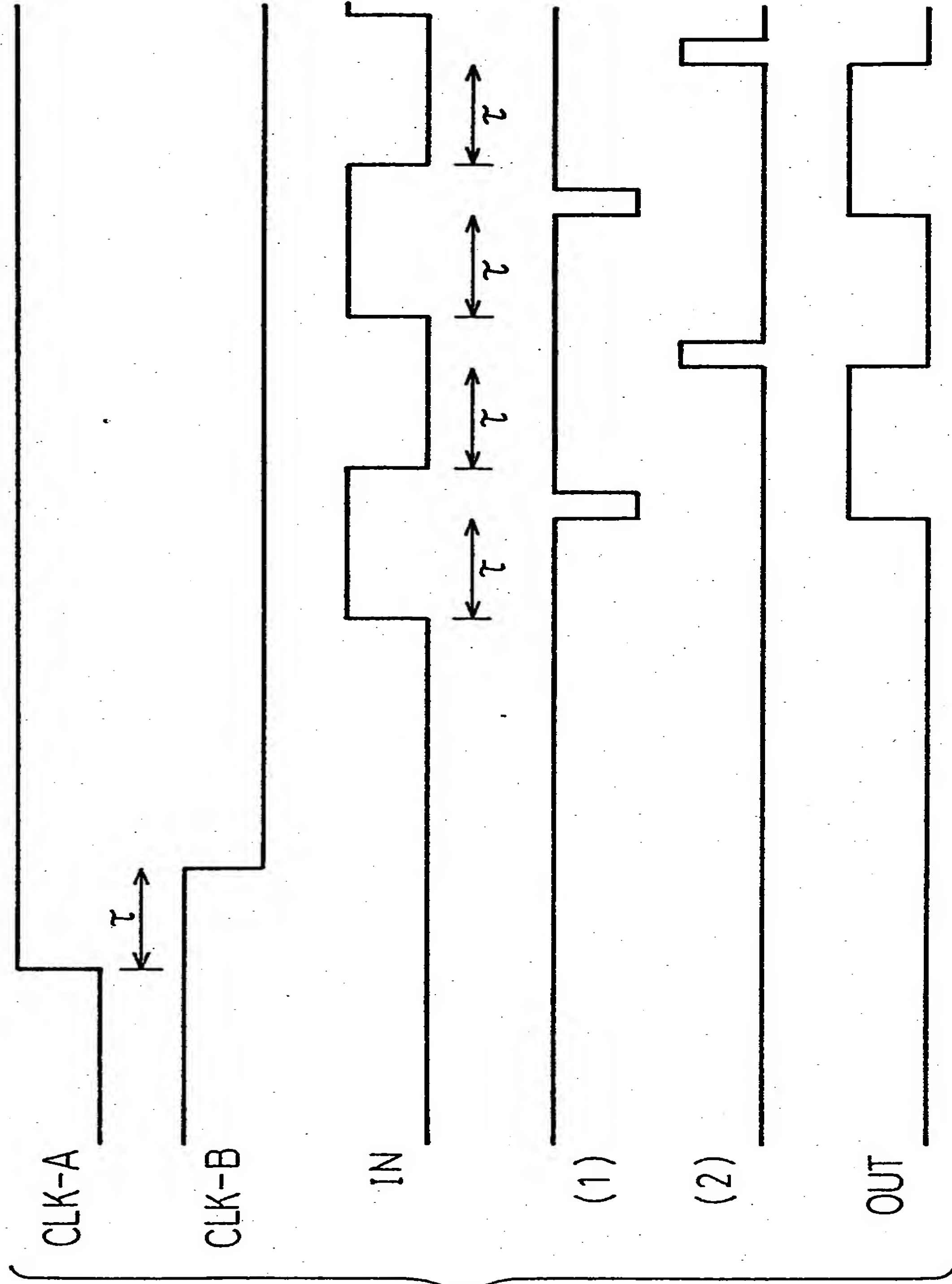


Fig.31

Fig. 32A

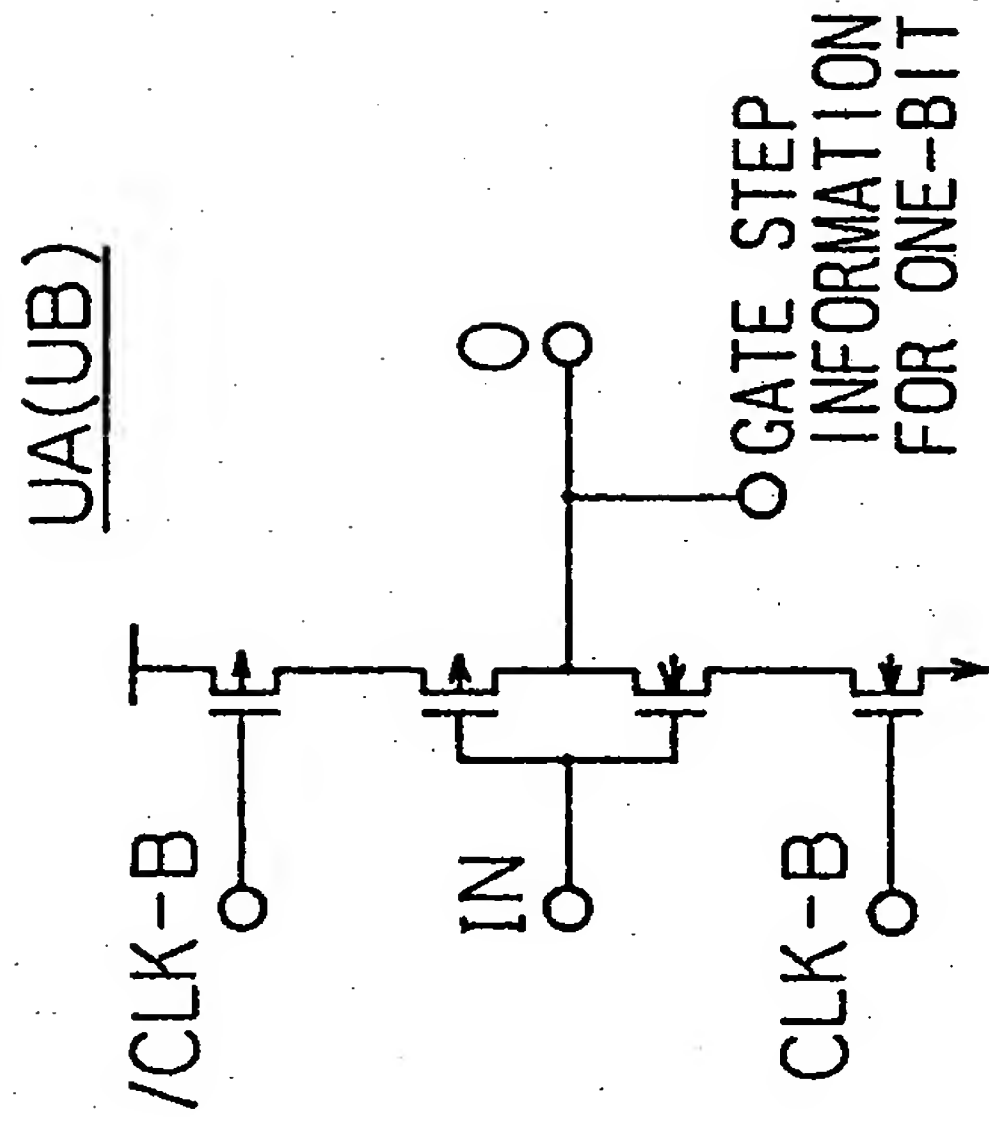


Fig. 32B

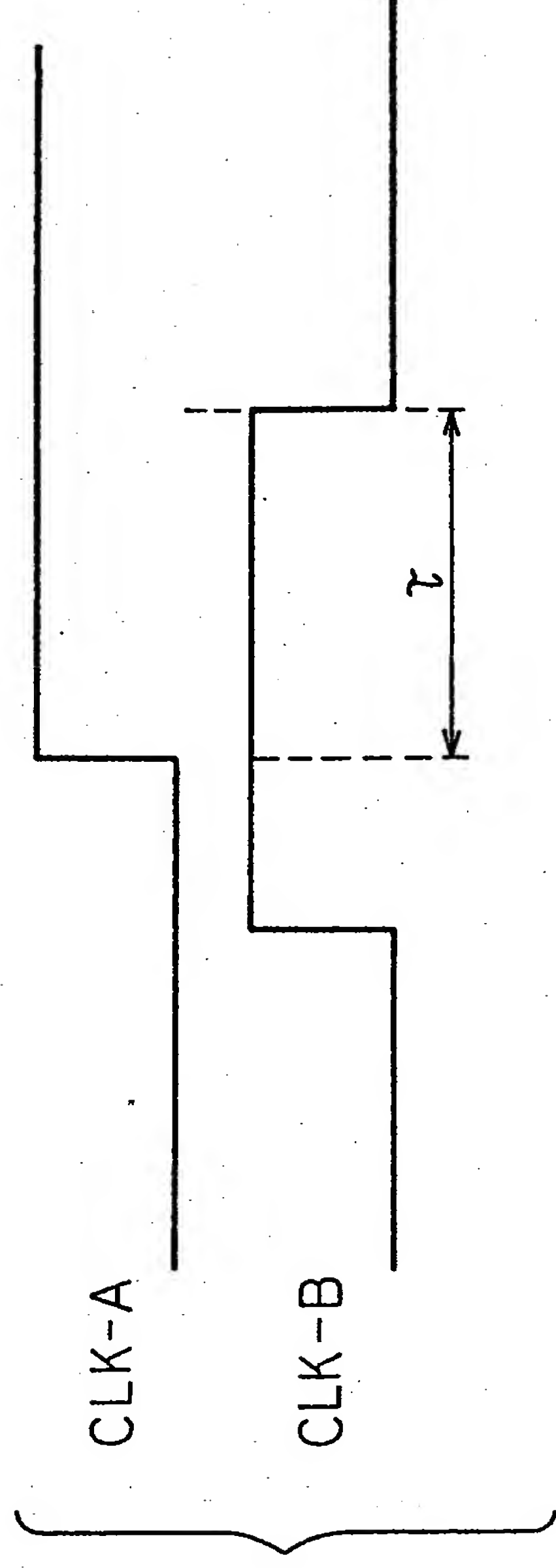
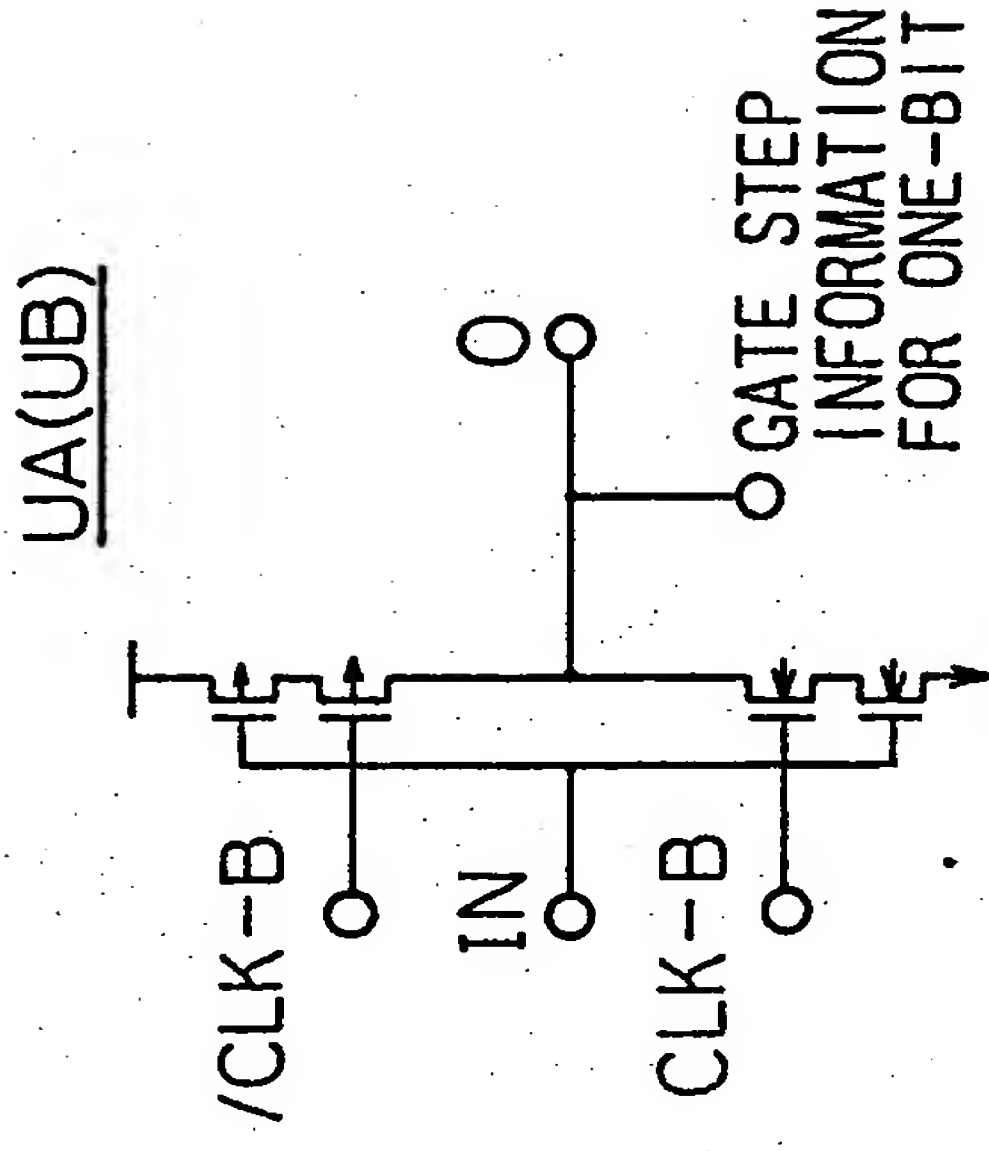


Fig. 32C

Fig. 33A

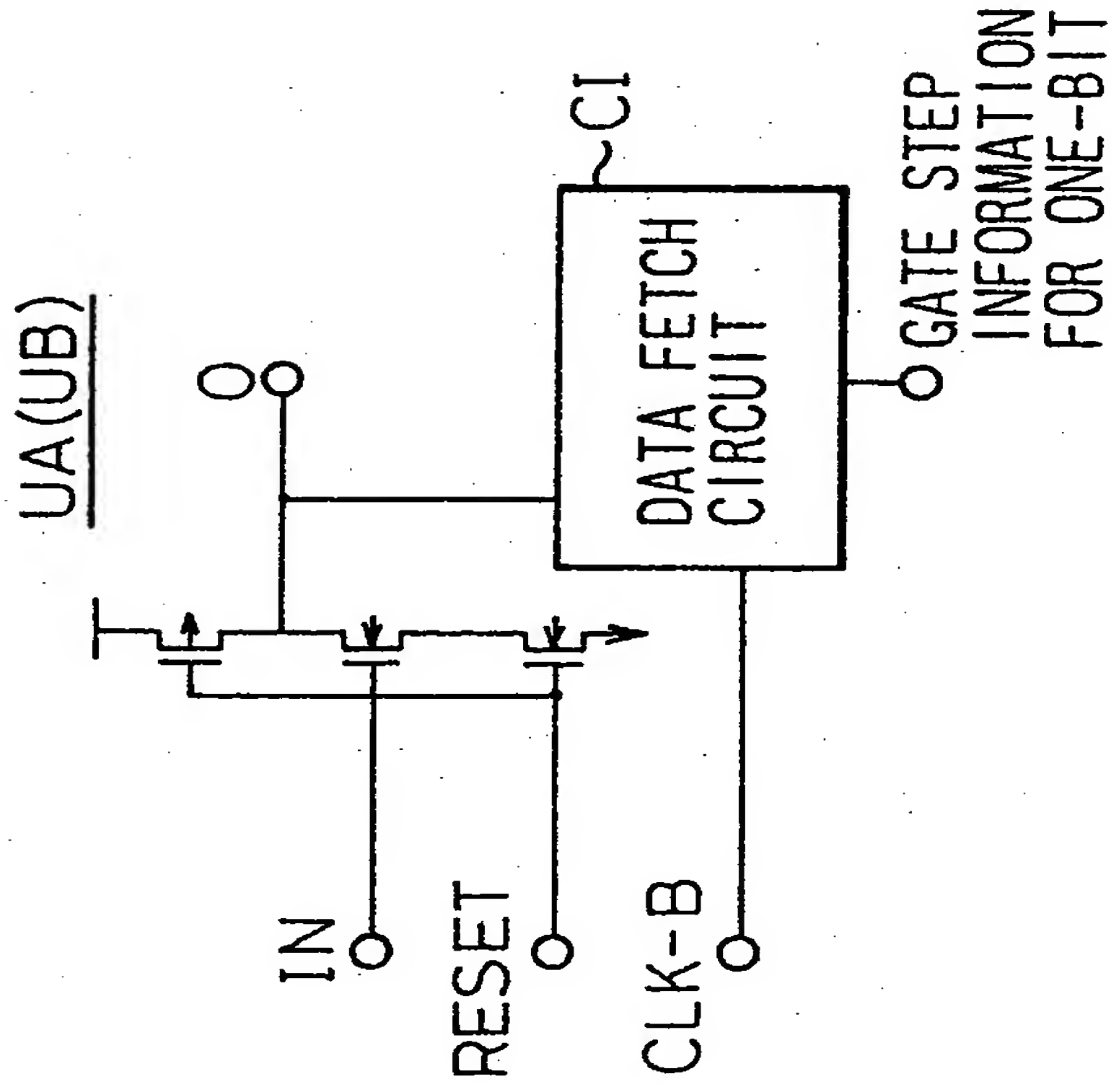


Fig. 33B

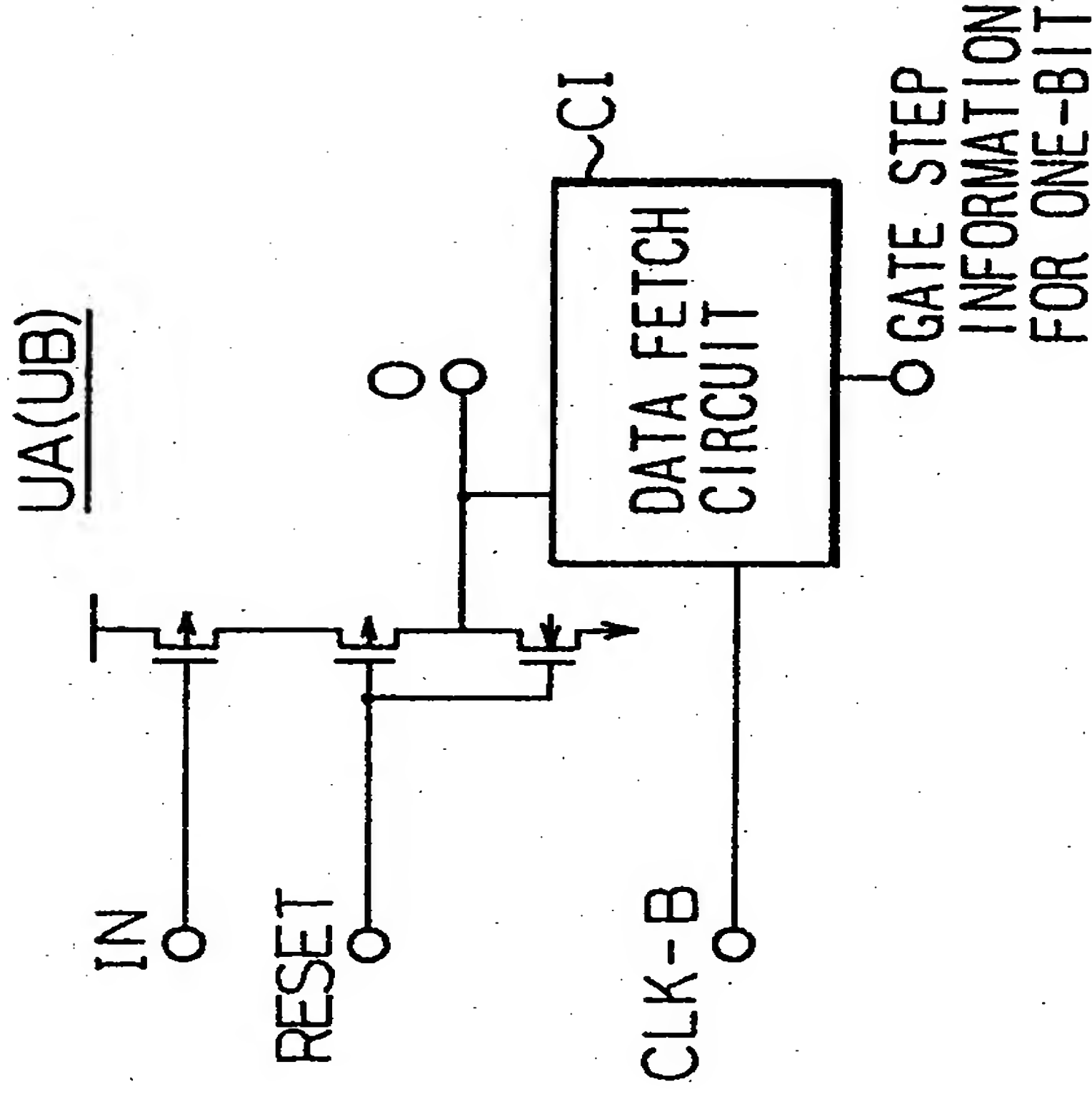


Fig. 34A

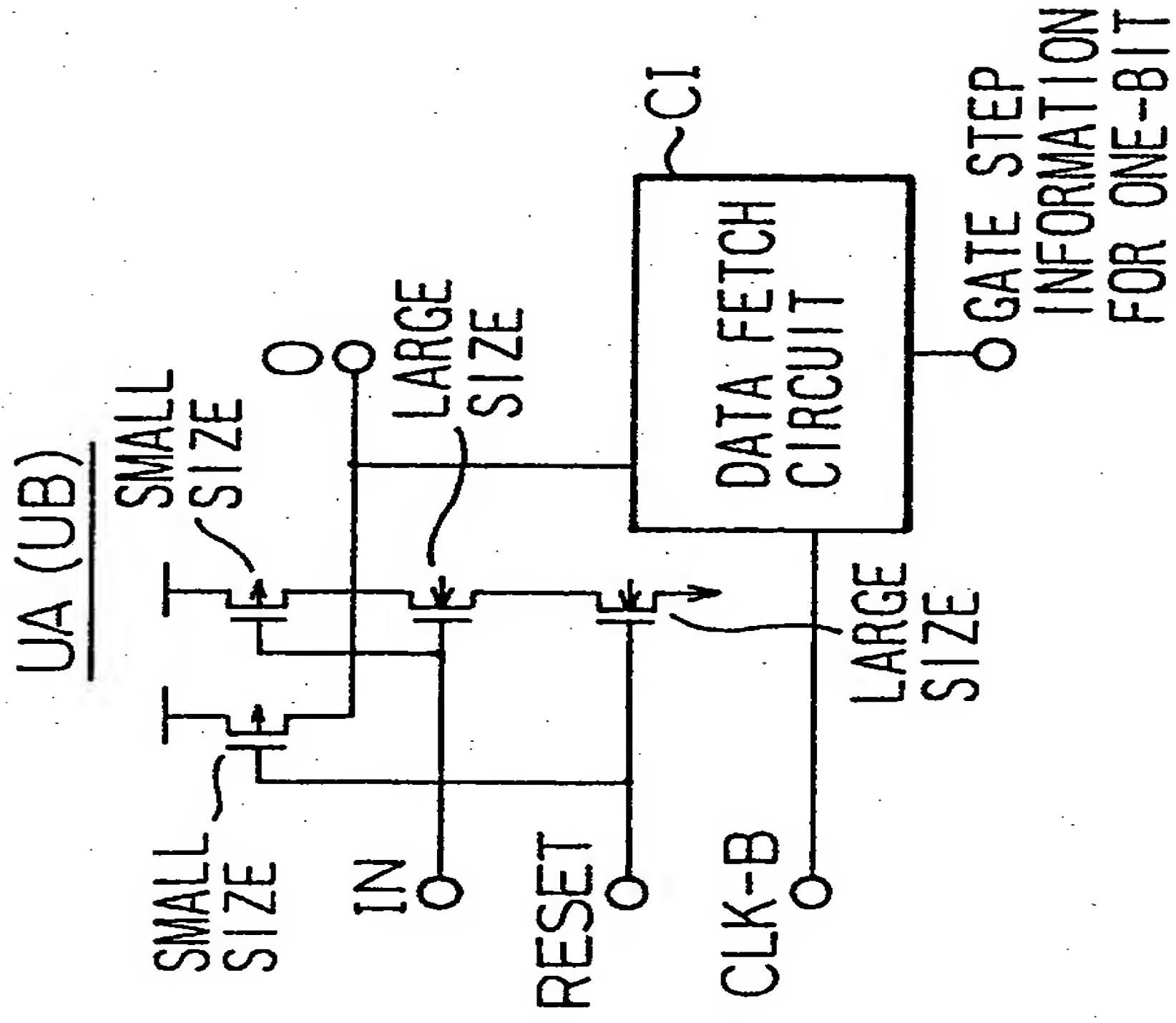


Fig. 34B

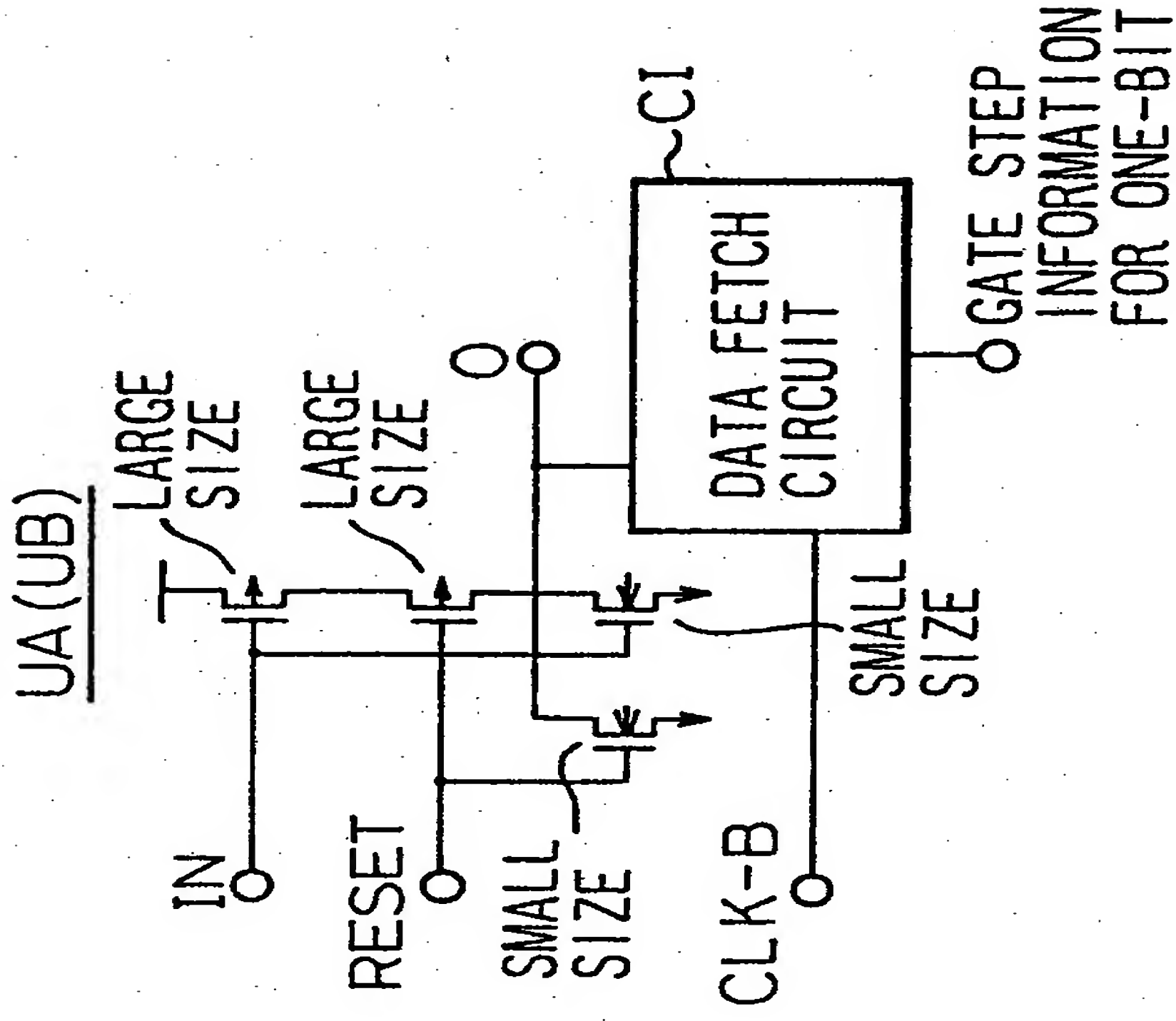


Fig. 35A

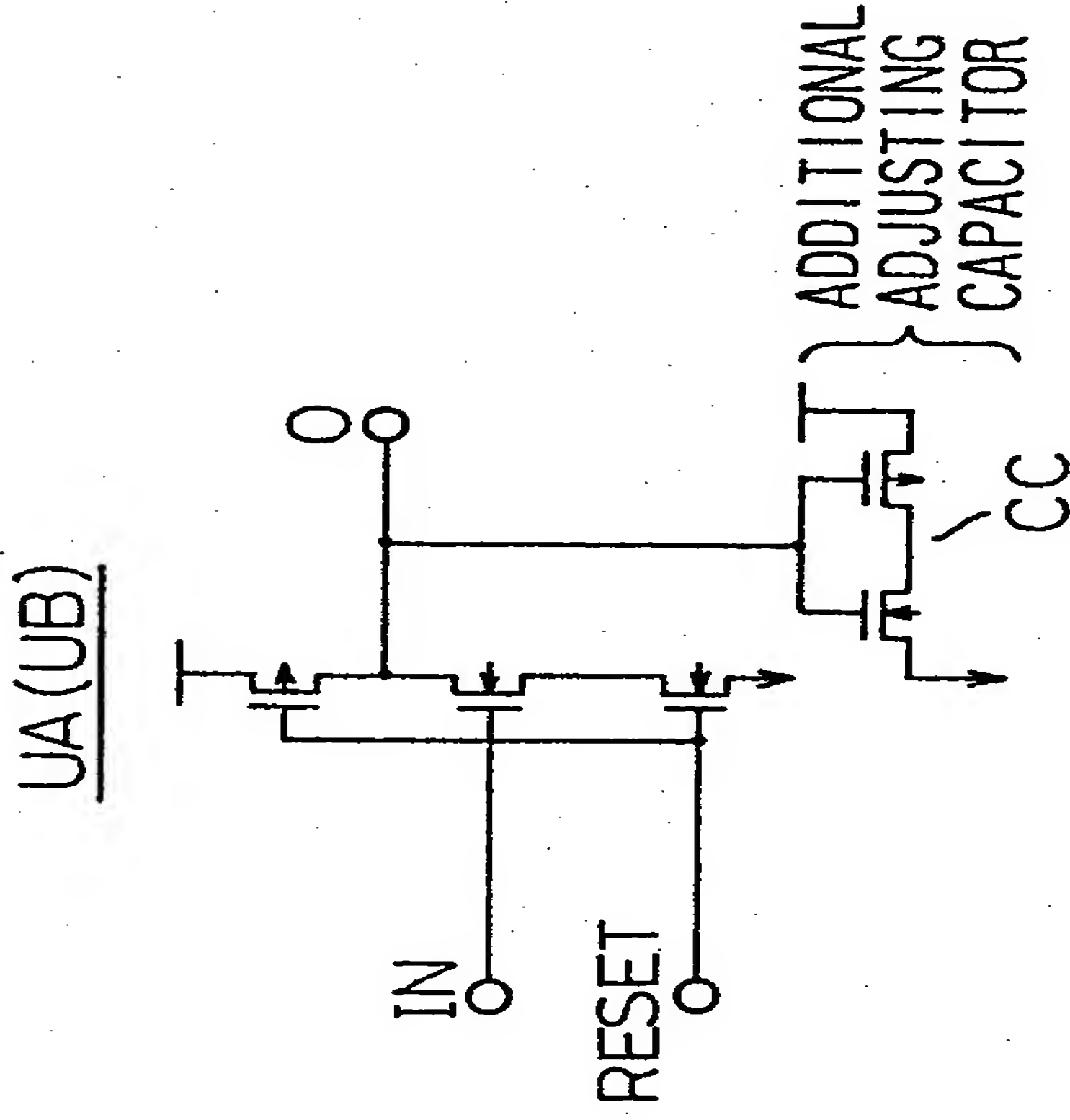


Fig. 35

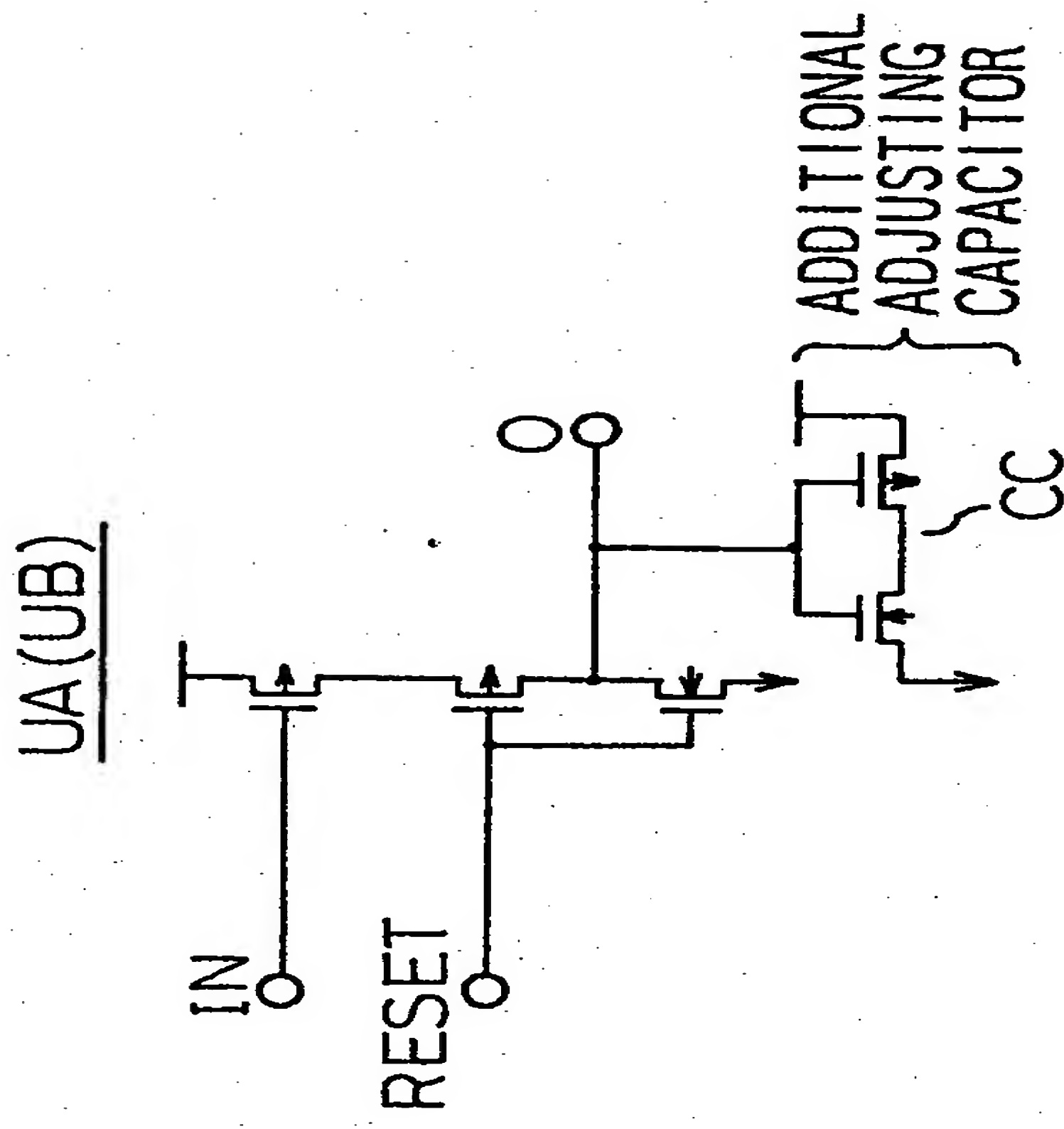


Fig. 36

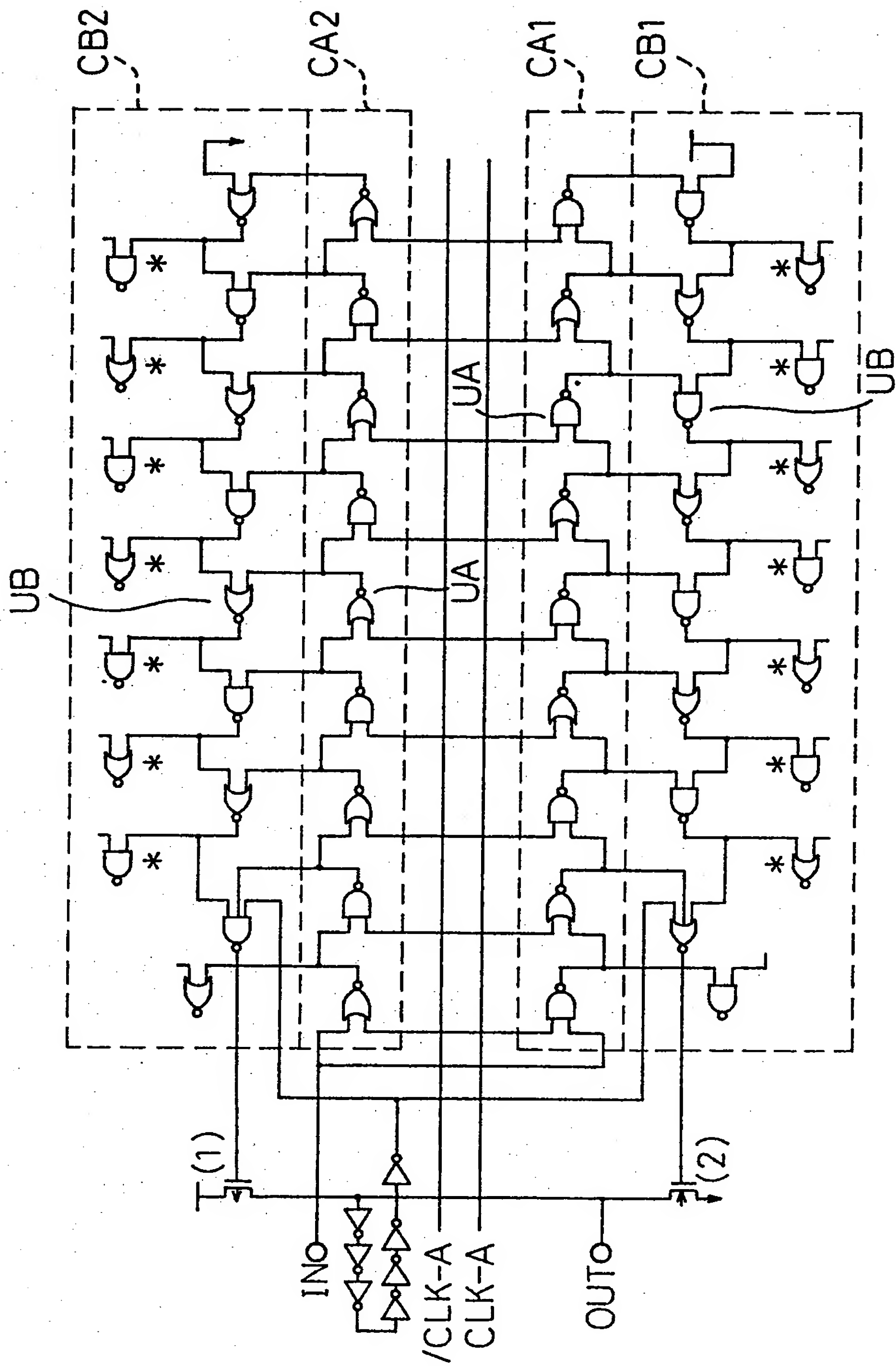


Fig. 37

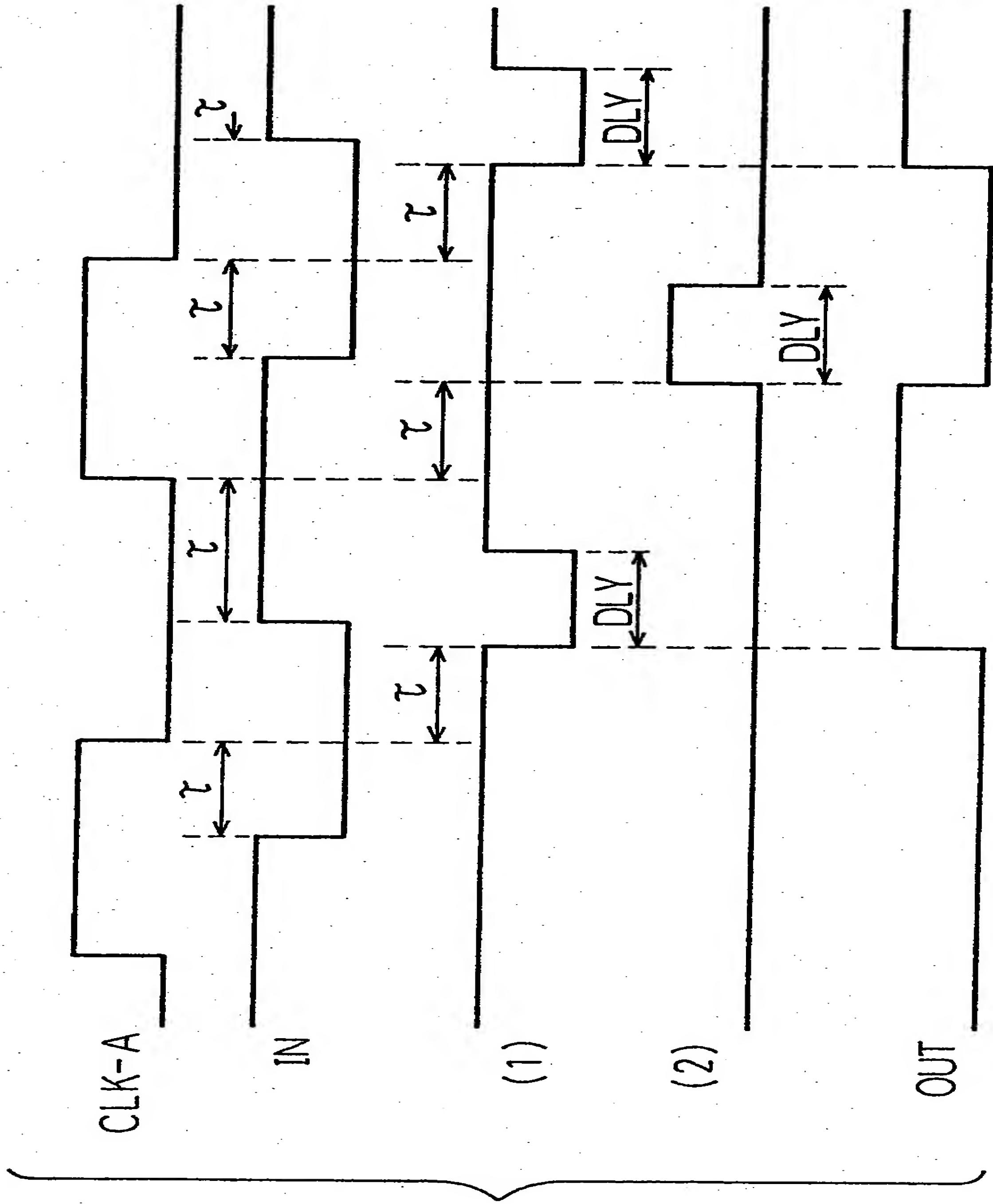


Fig. 38A

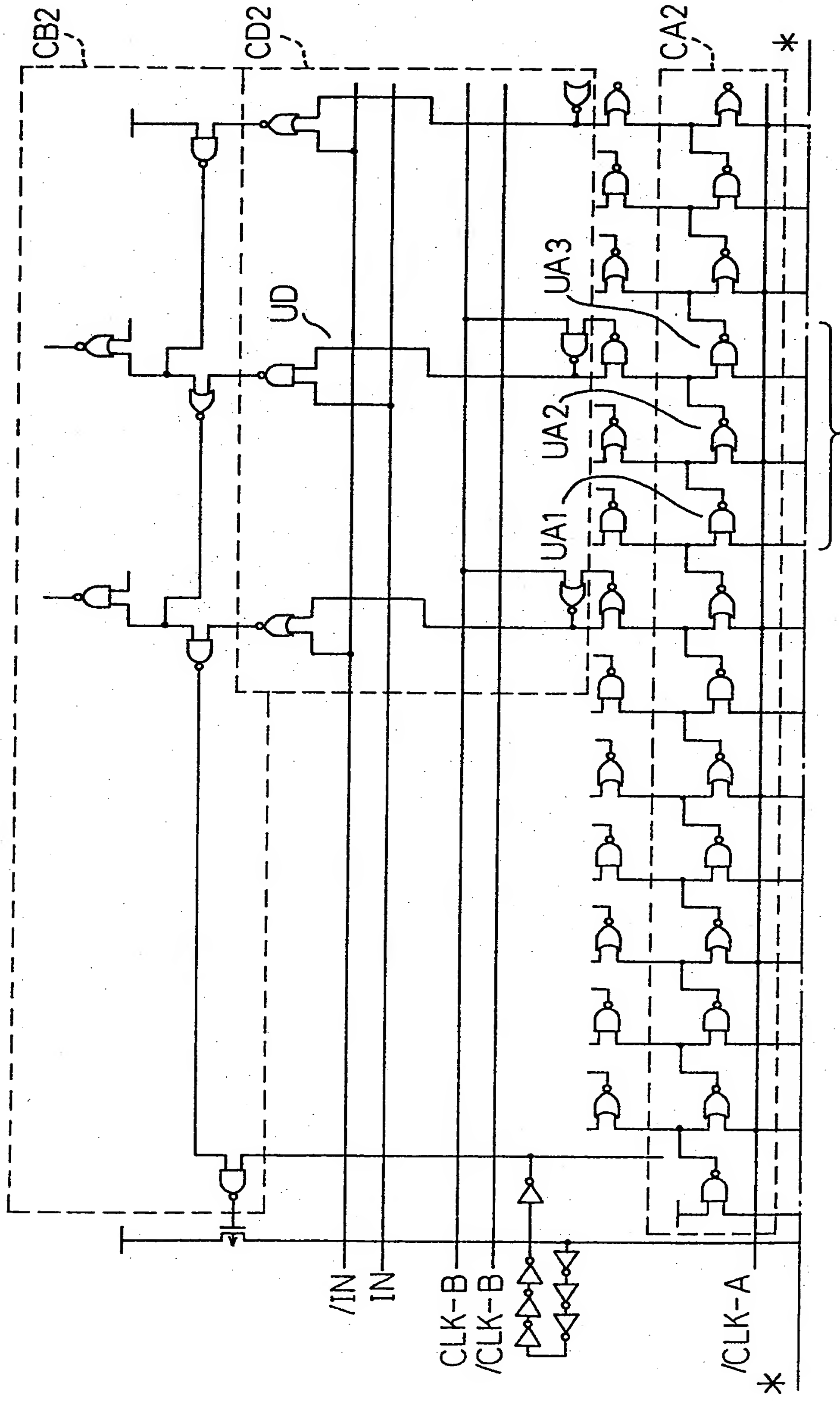
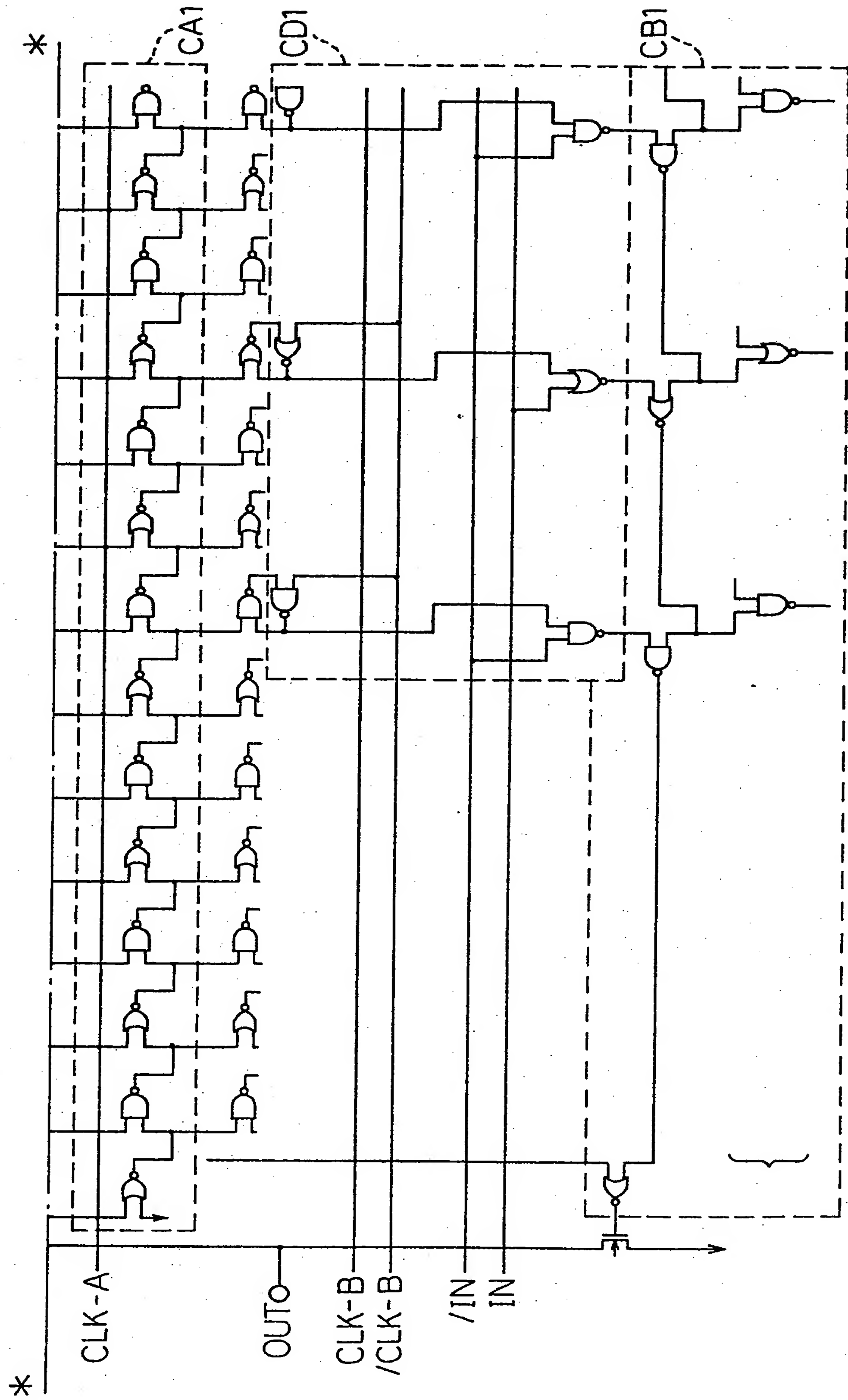


Fig. 38B



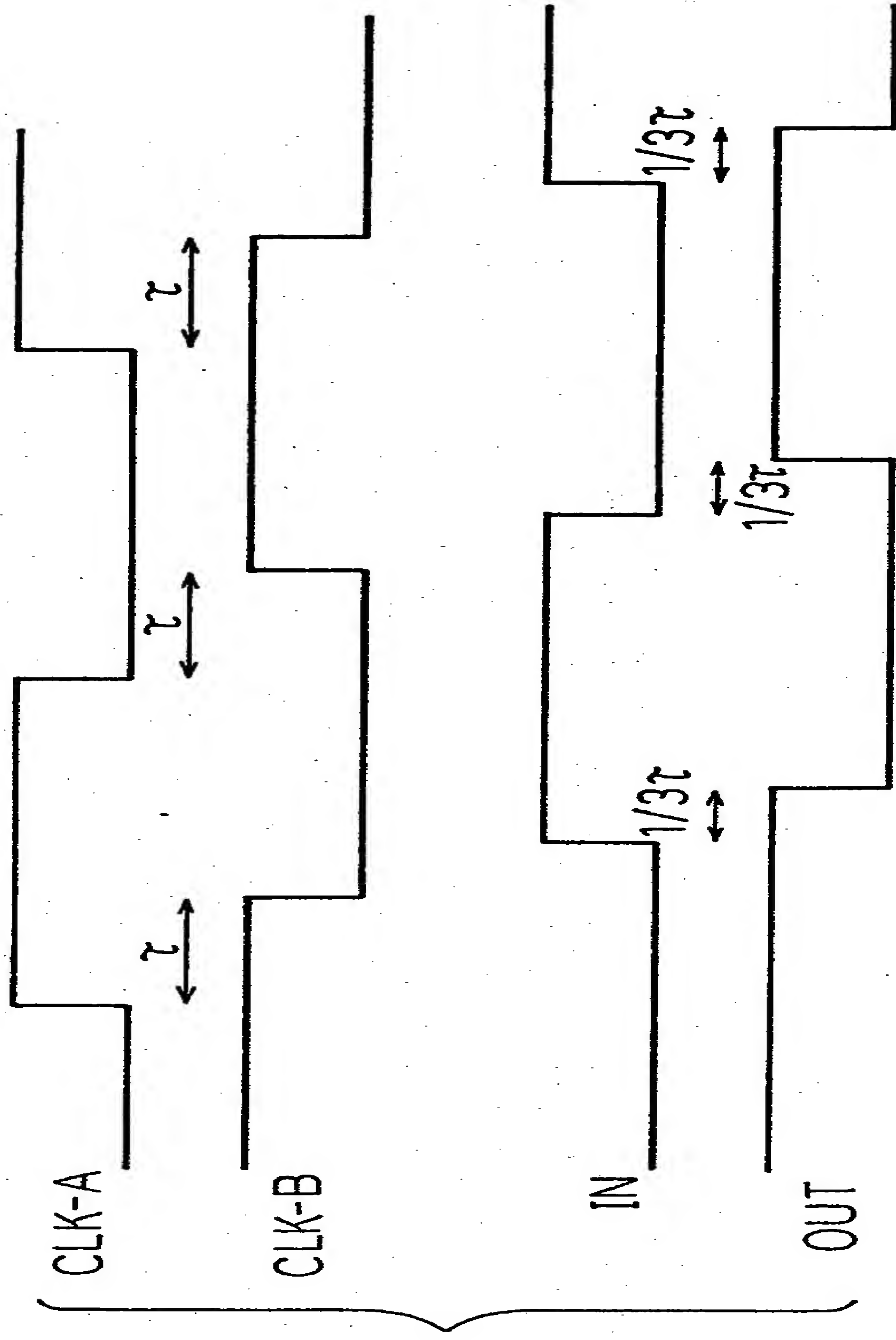


Fig. 39

Fig. 40A

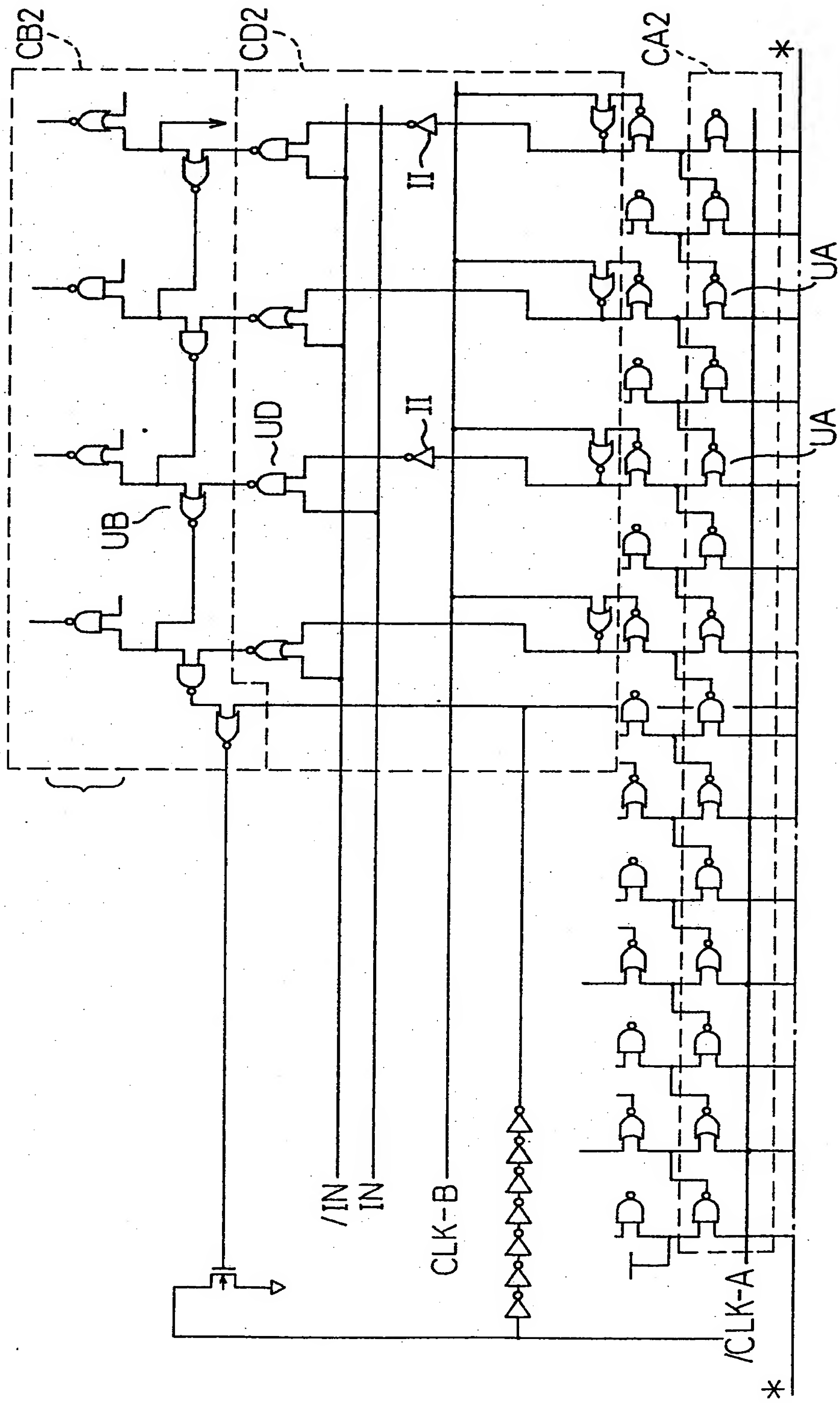
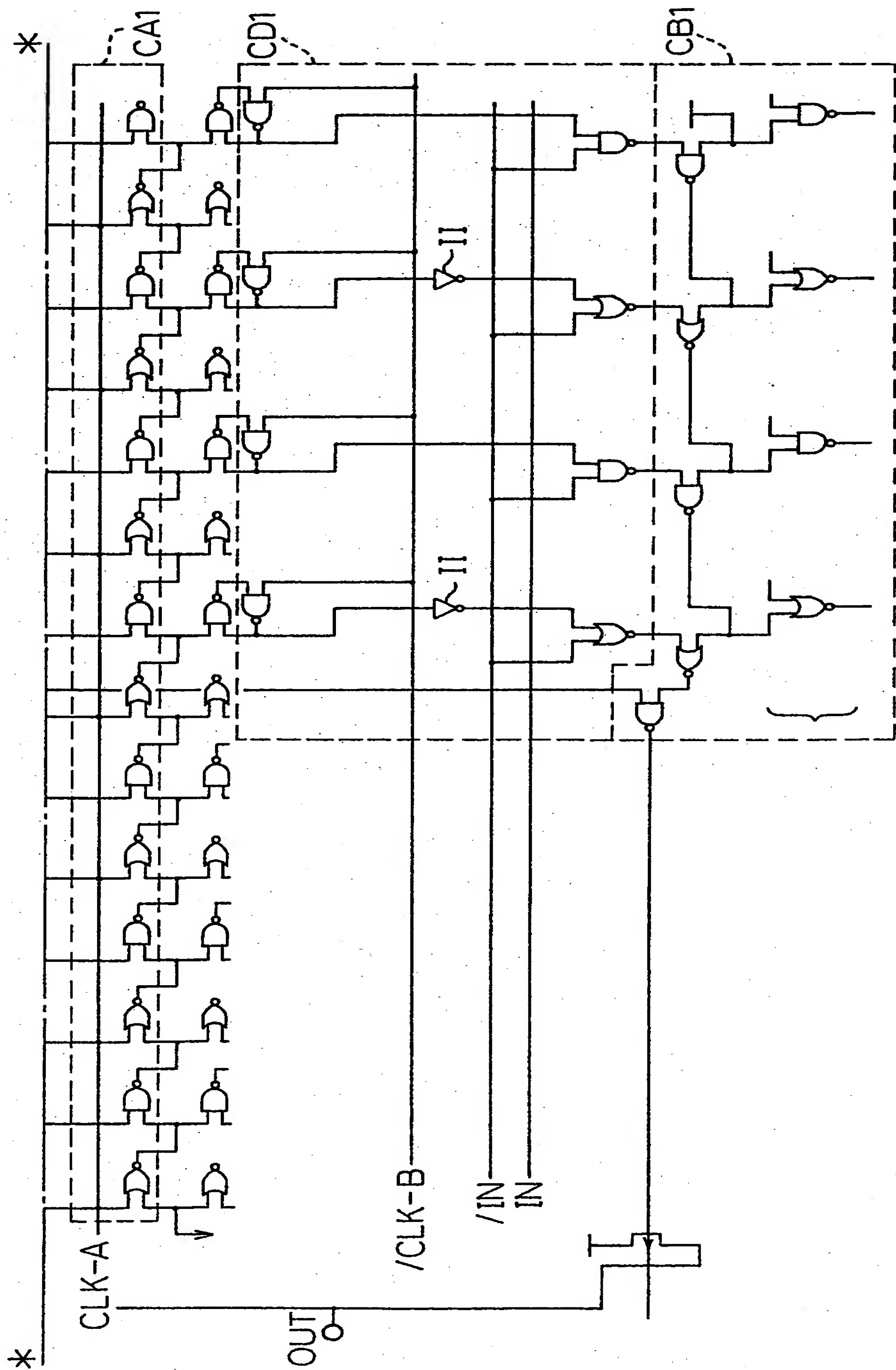


Fig. 40B



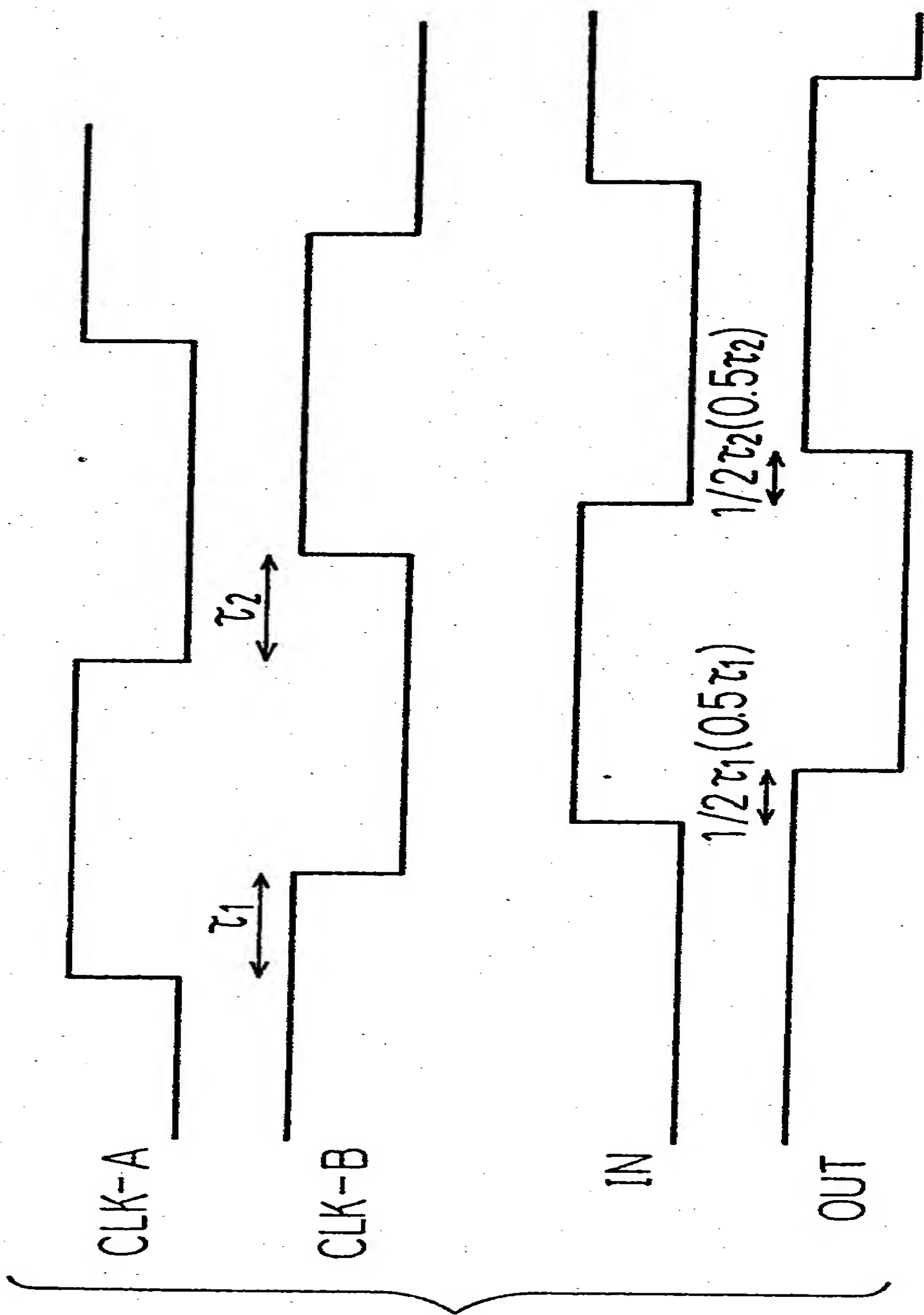


Fig. 41

Fig. 42A

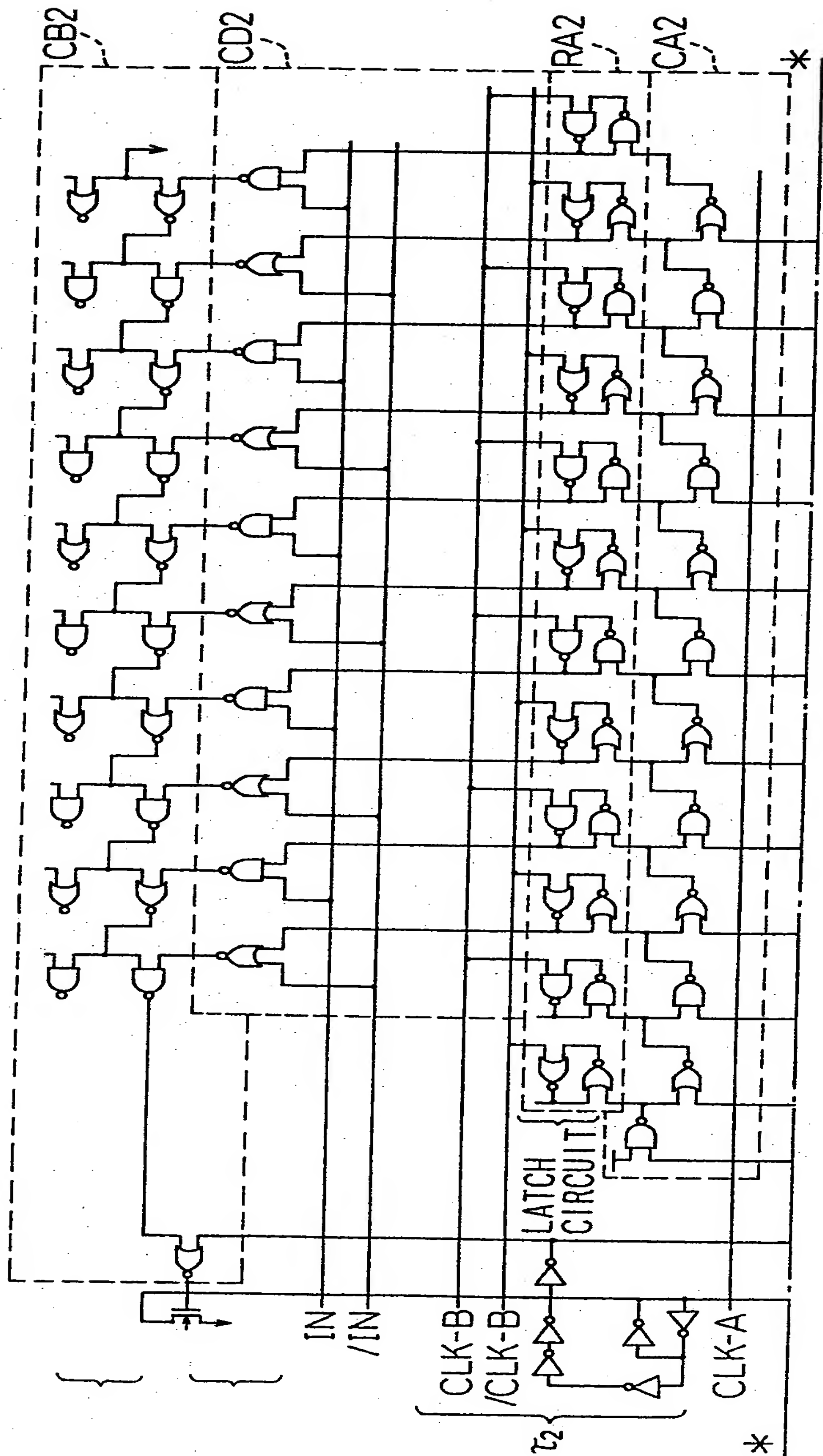
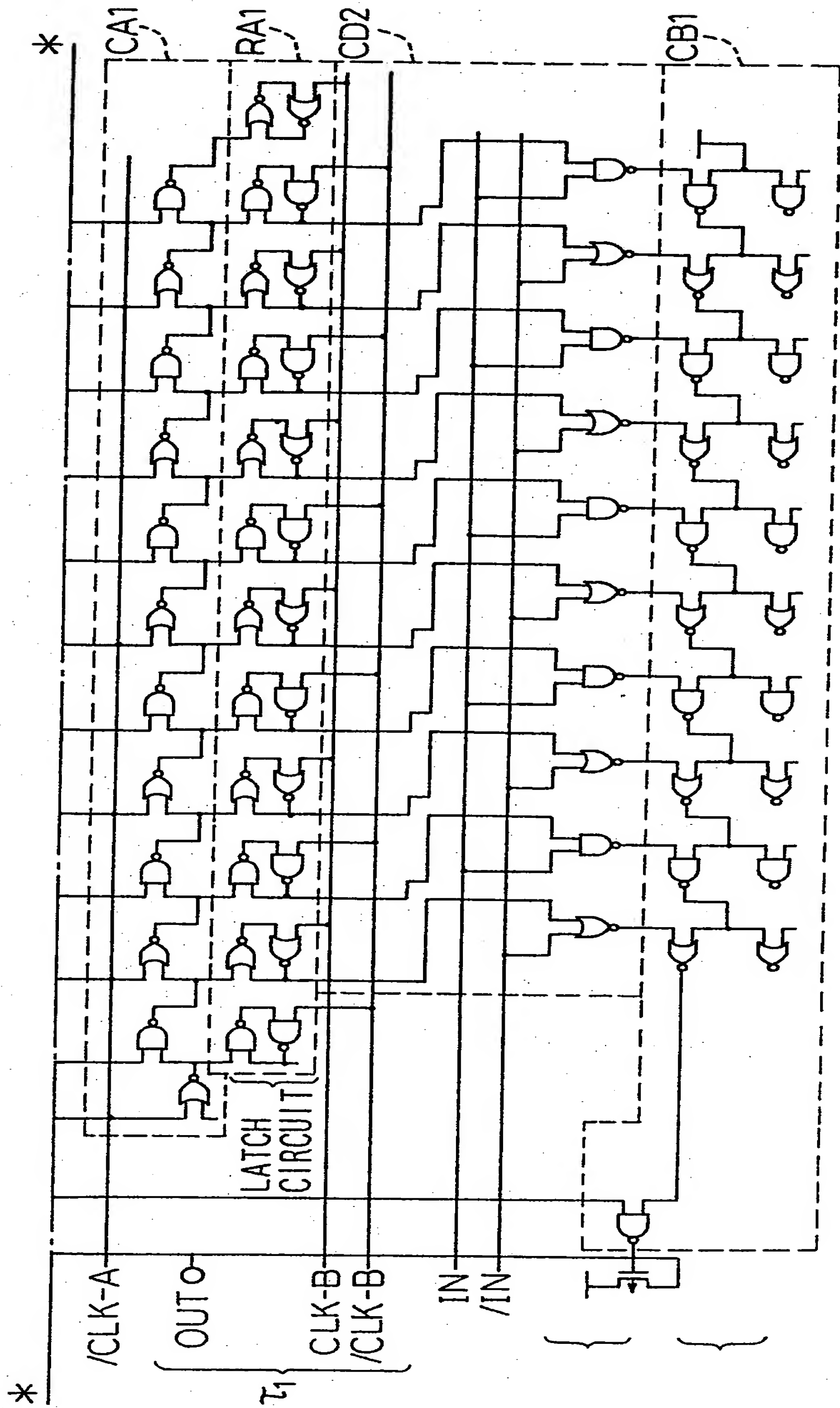


Fig. 42B



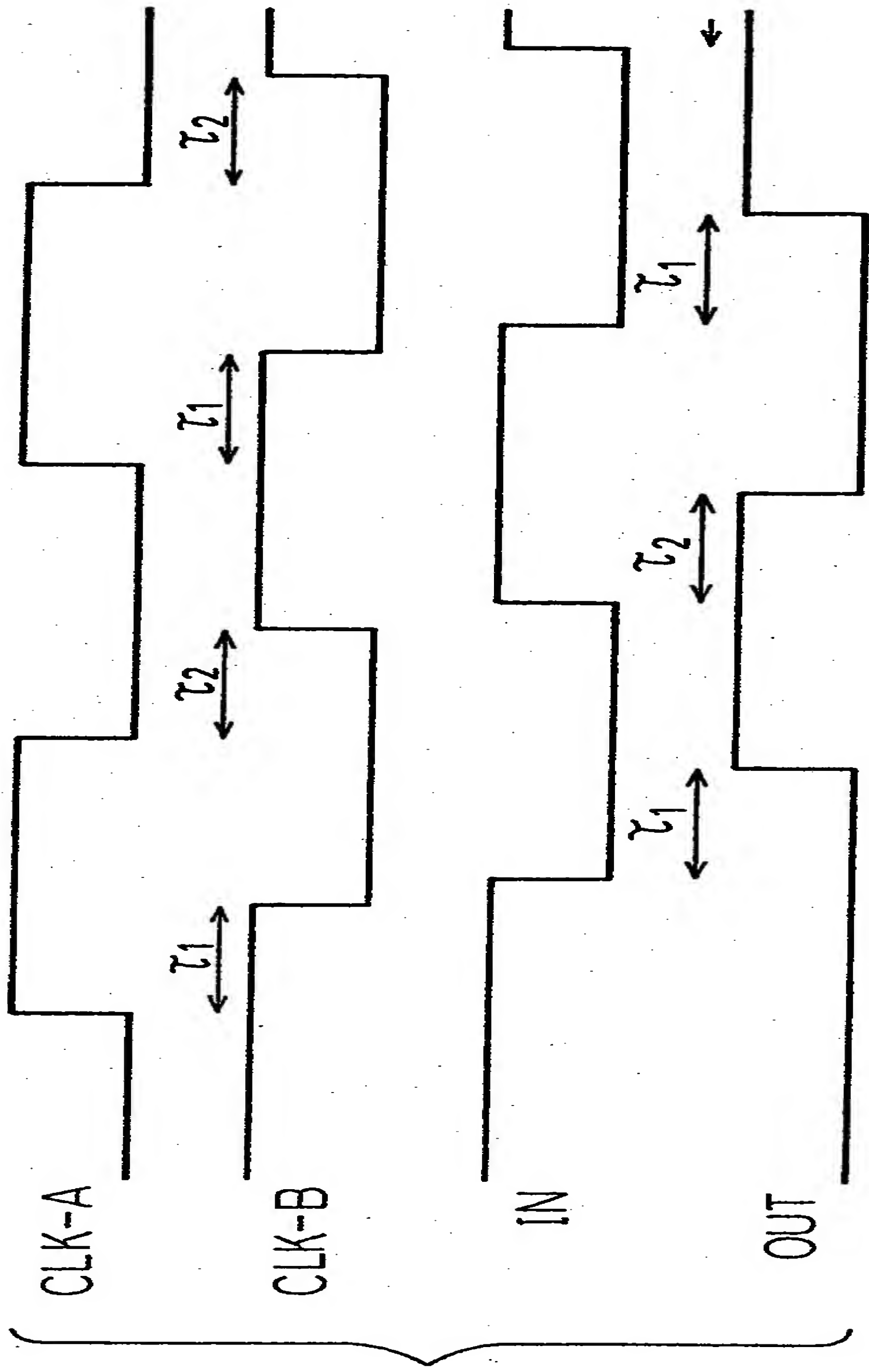


Fig. 43

Fig. 44A

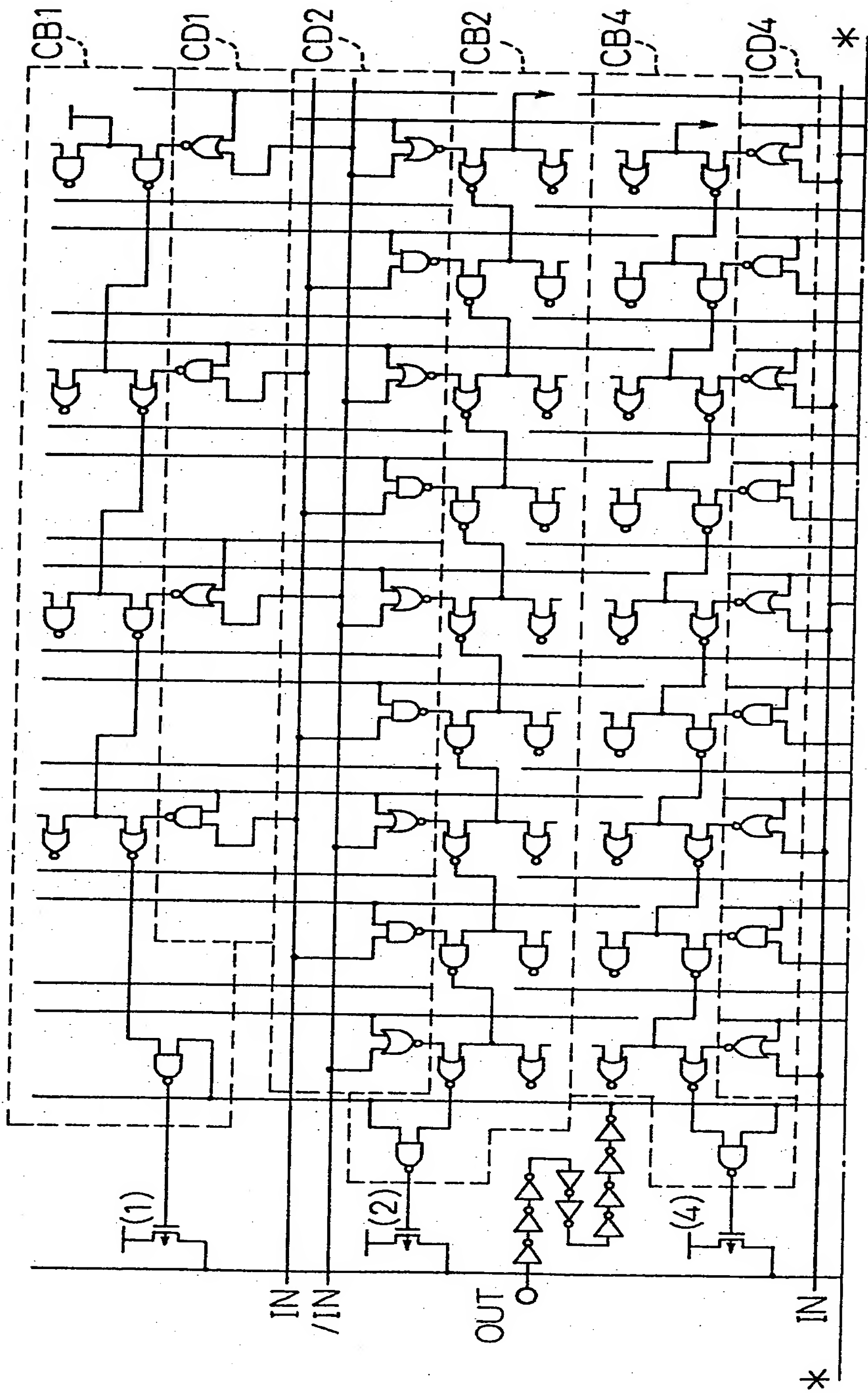


Fig. 44B

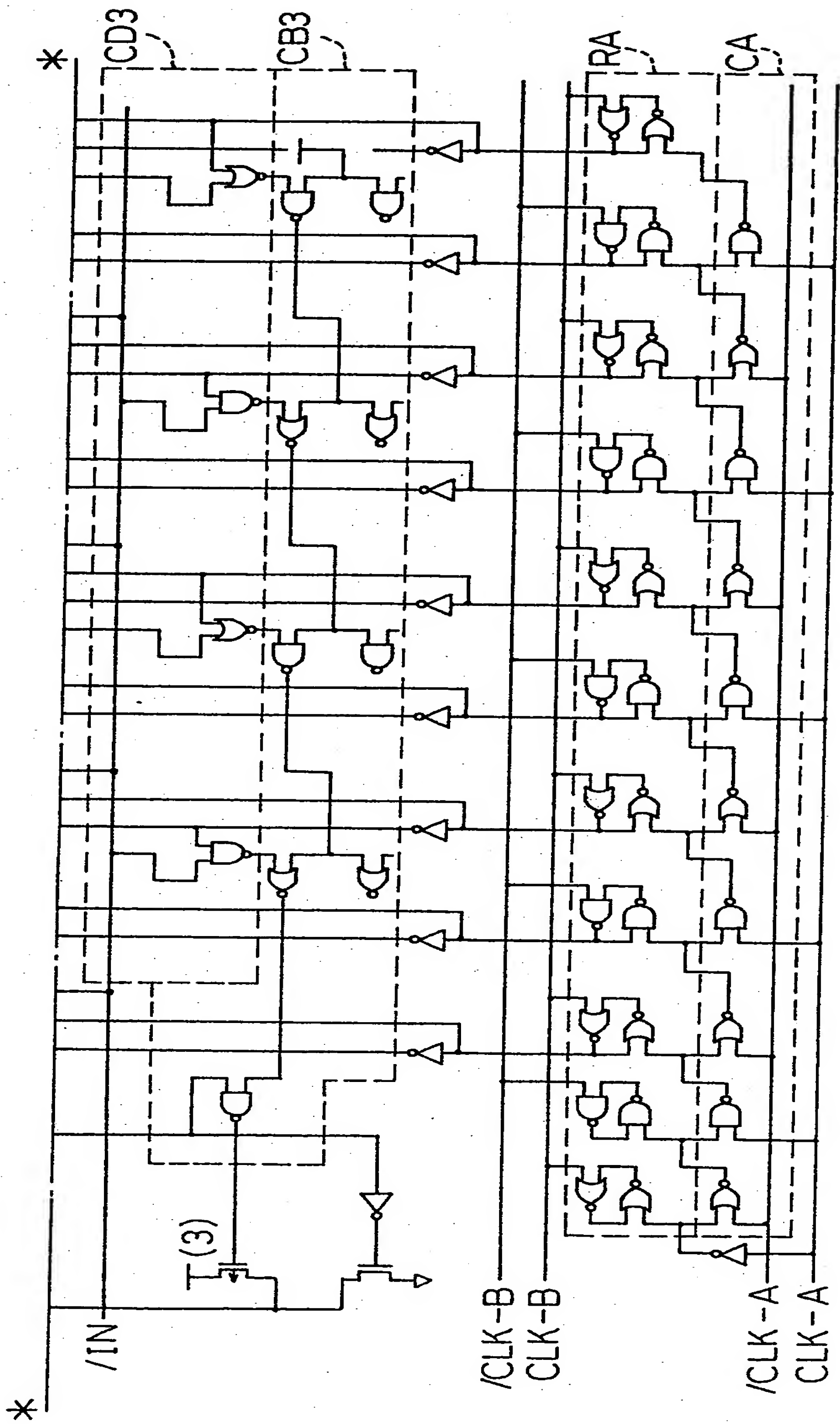


Fig. 45

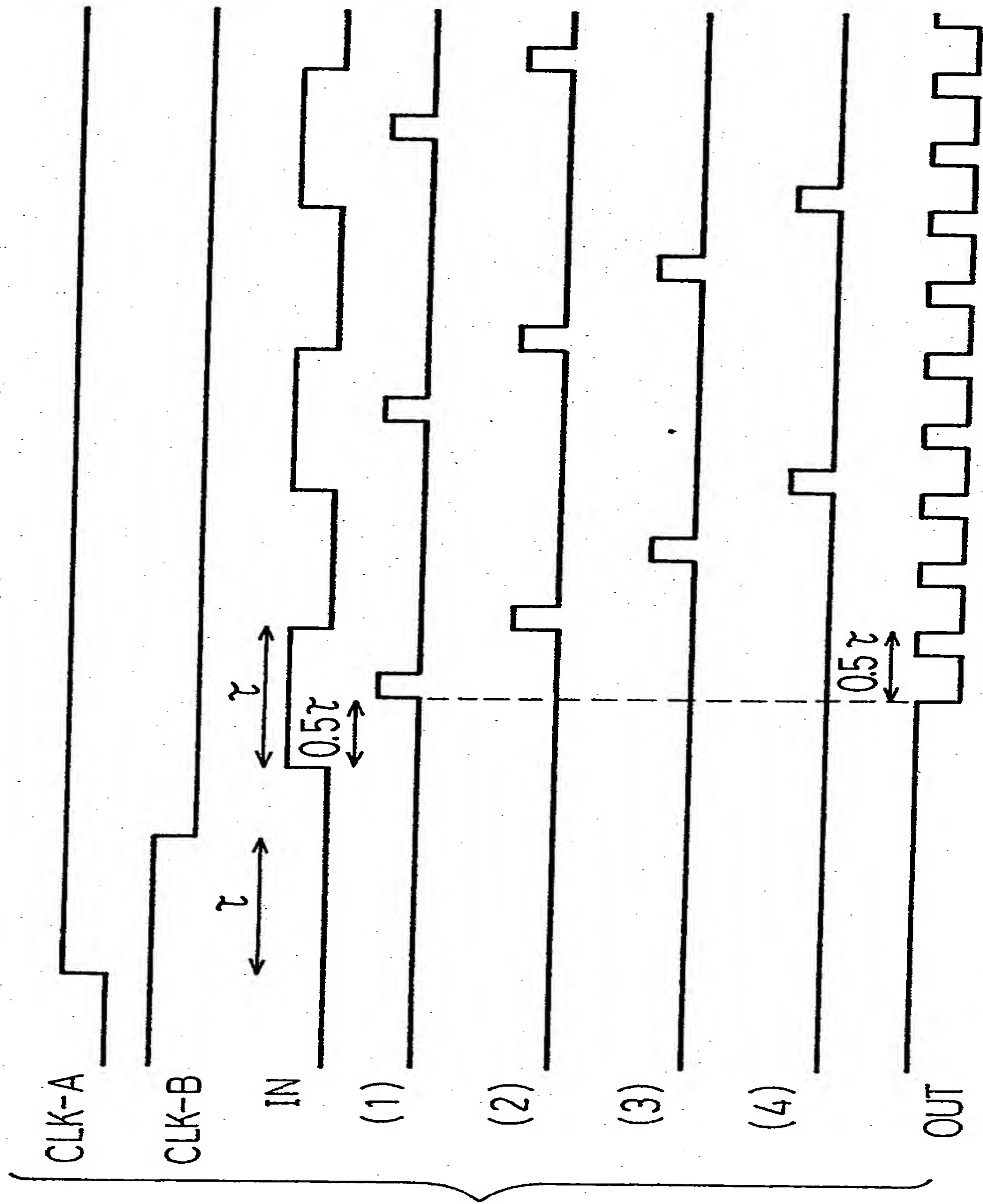


Fig. 46

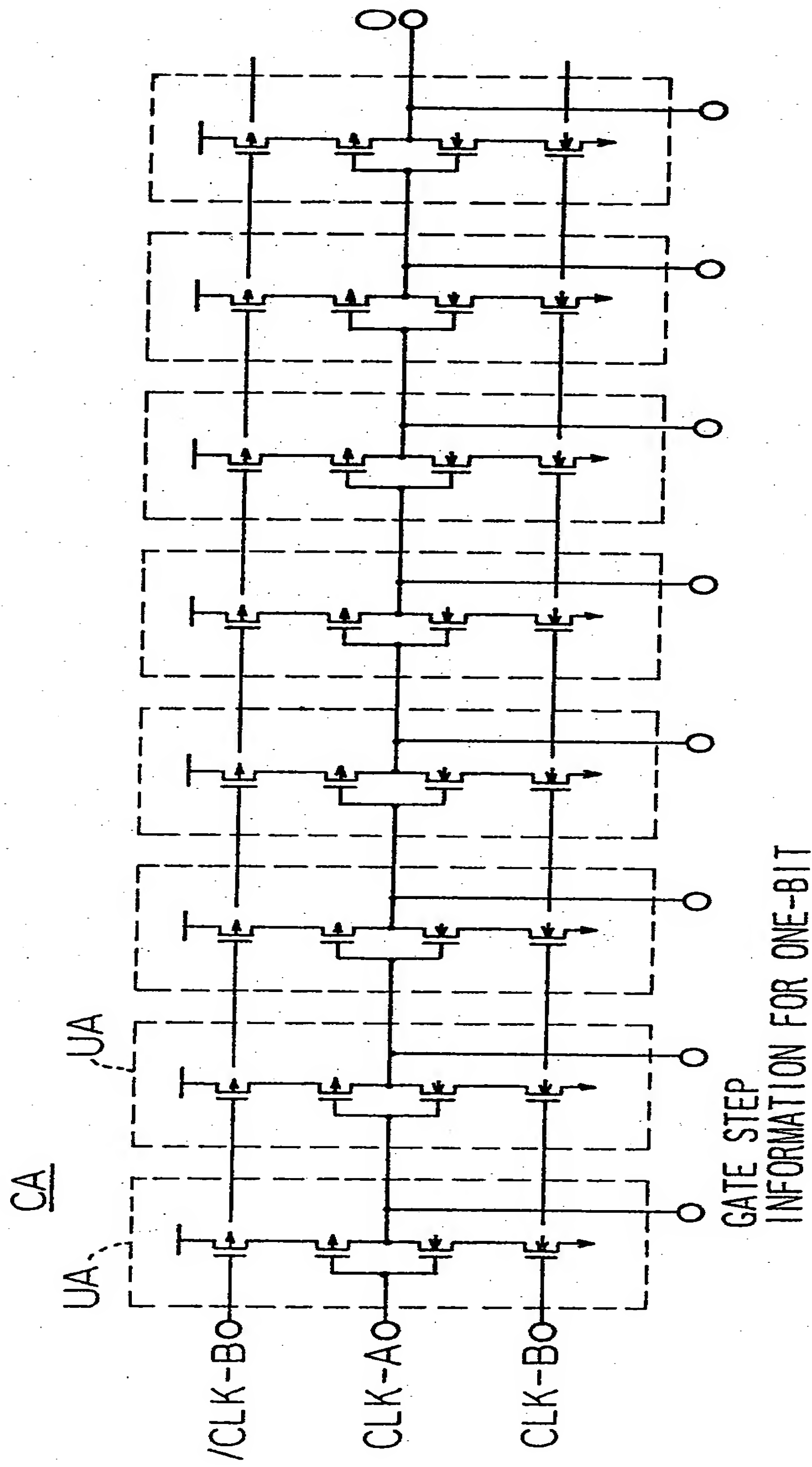


Fig. 47

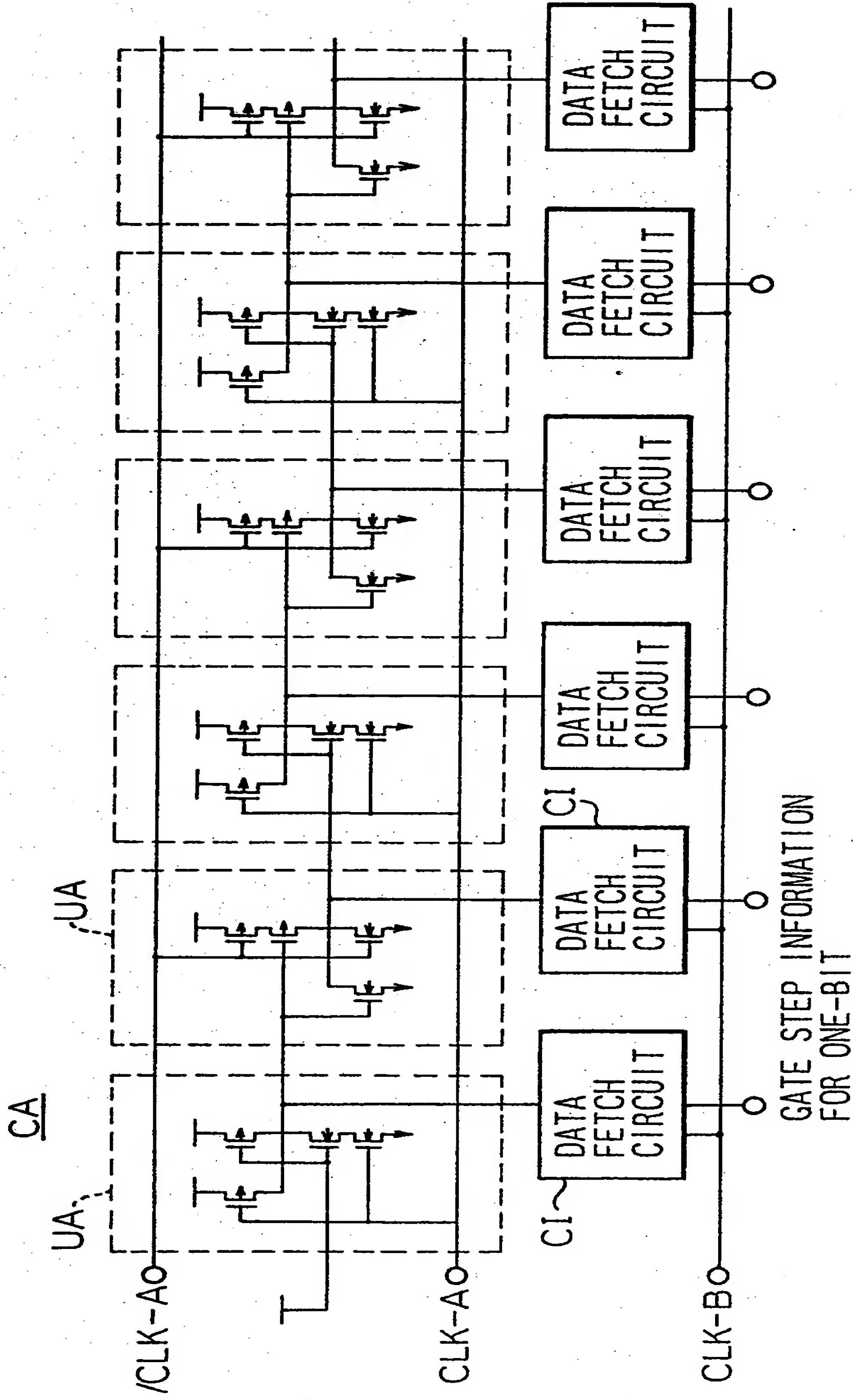


Fig. 48

CB

GATE STEP INFORMATION (N' -BIT)

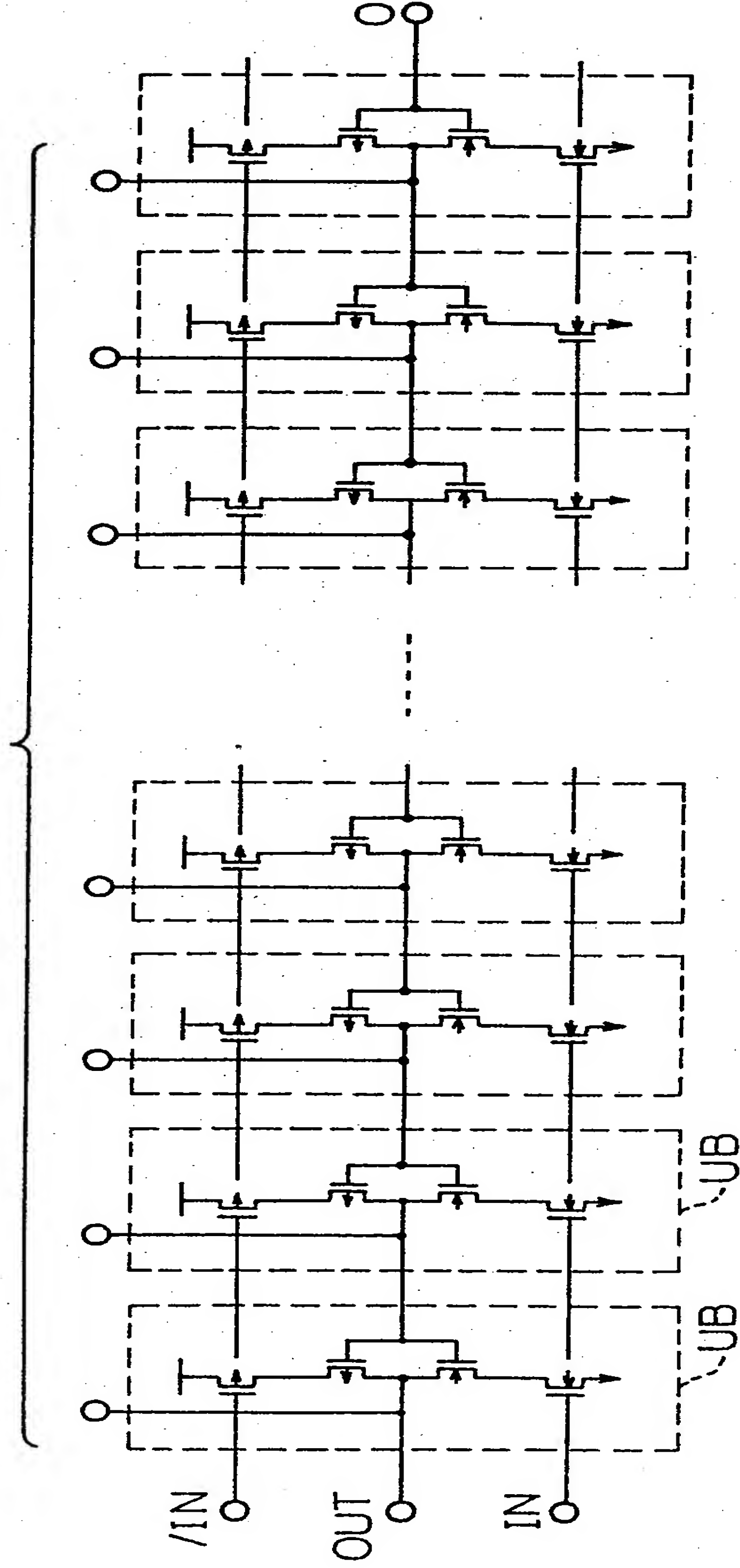


Fig. 49

CB

GATE STEP INFORMATION (N' -BIT)

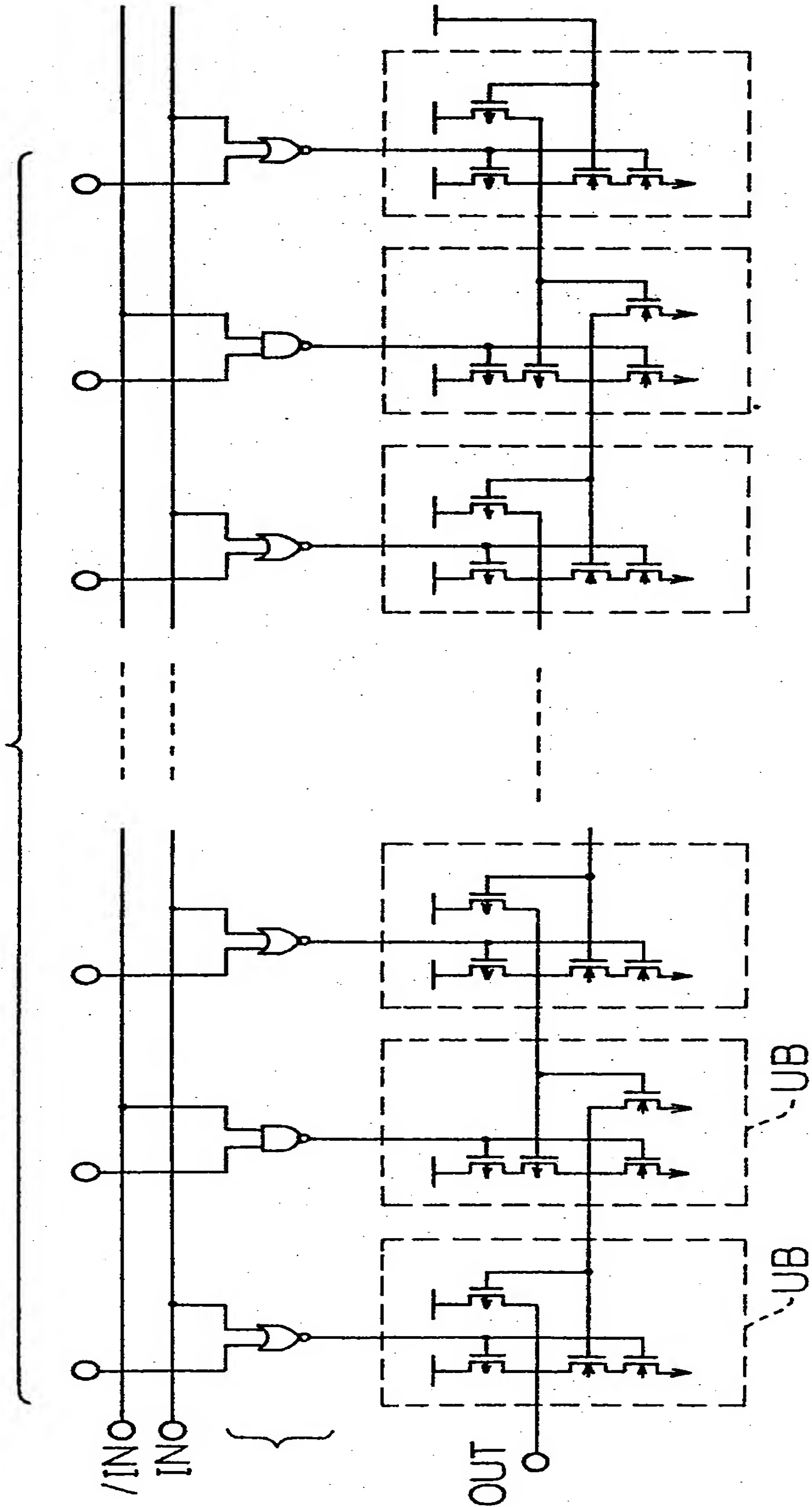


Fig. 50A

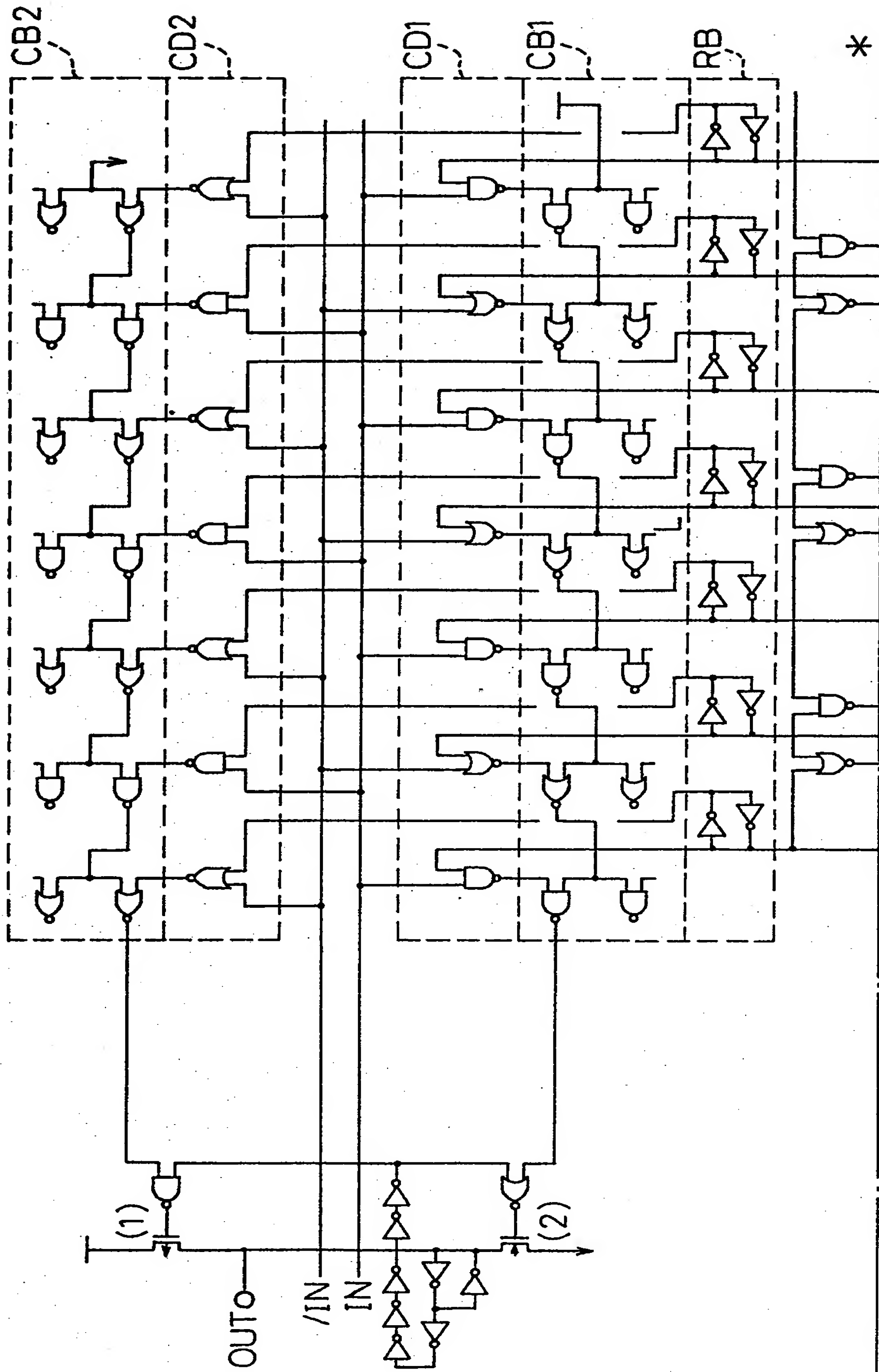
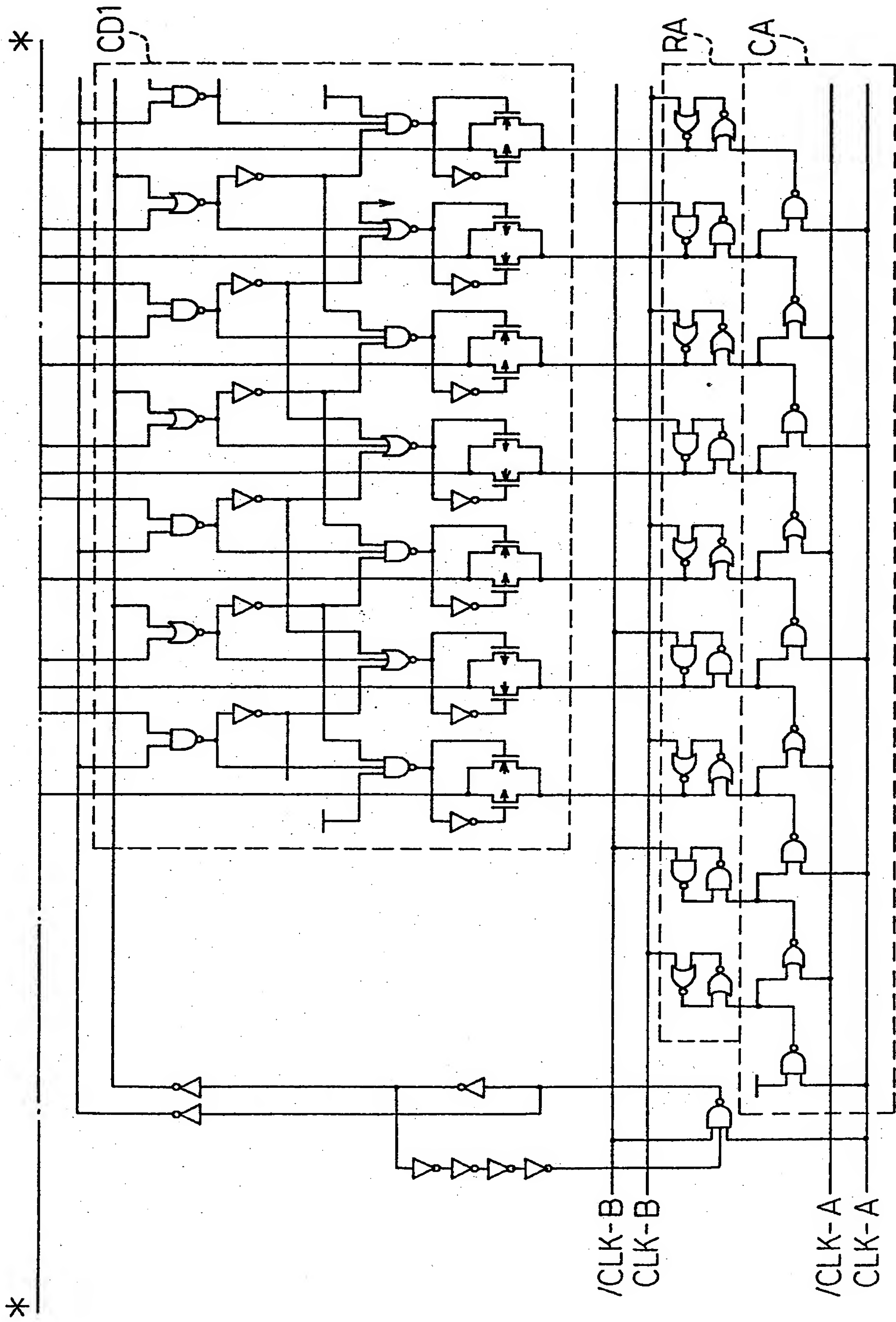


Fig. 50B



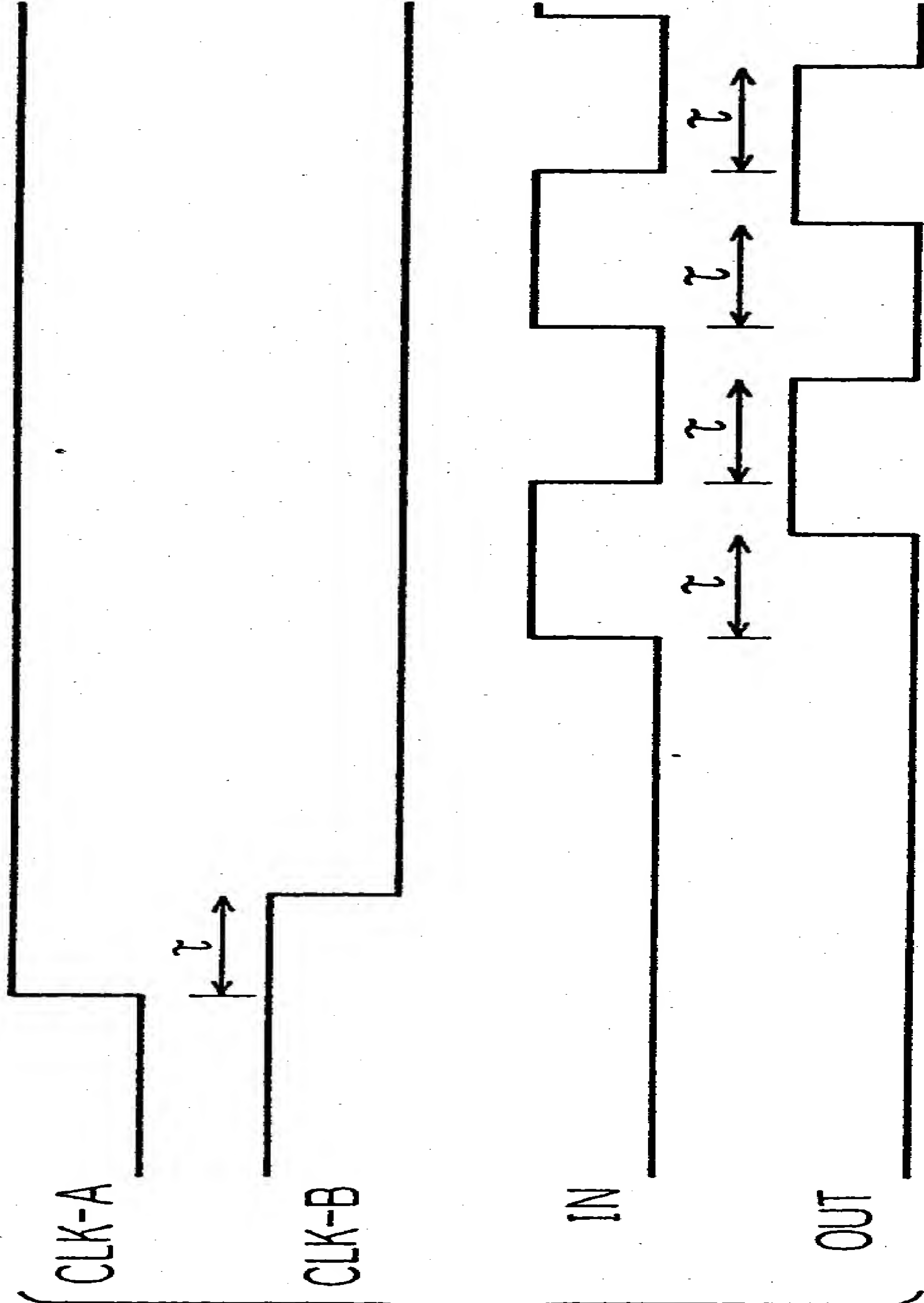


Fig. 51

Fig. 52A

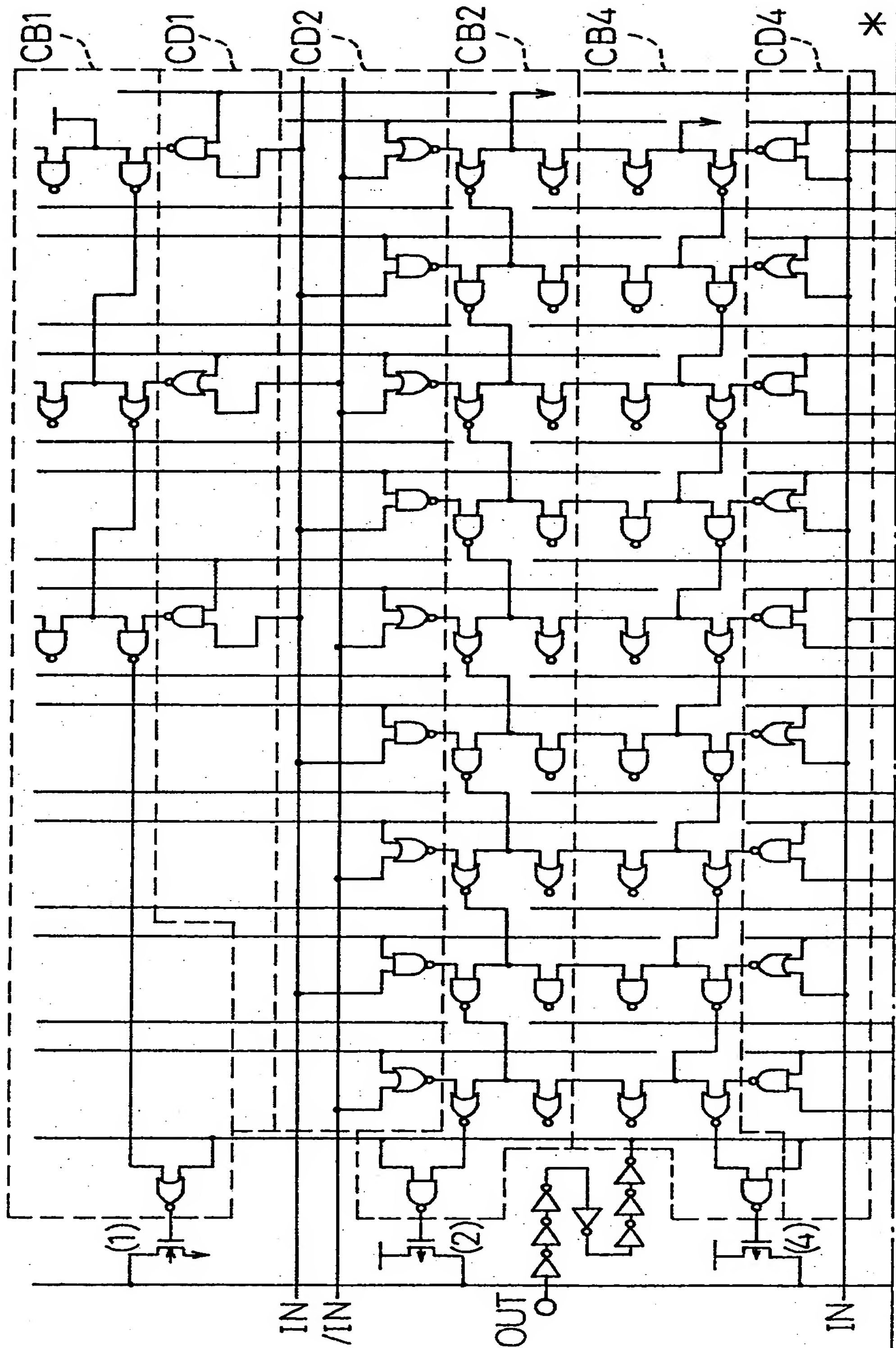
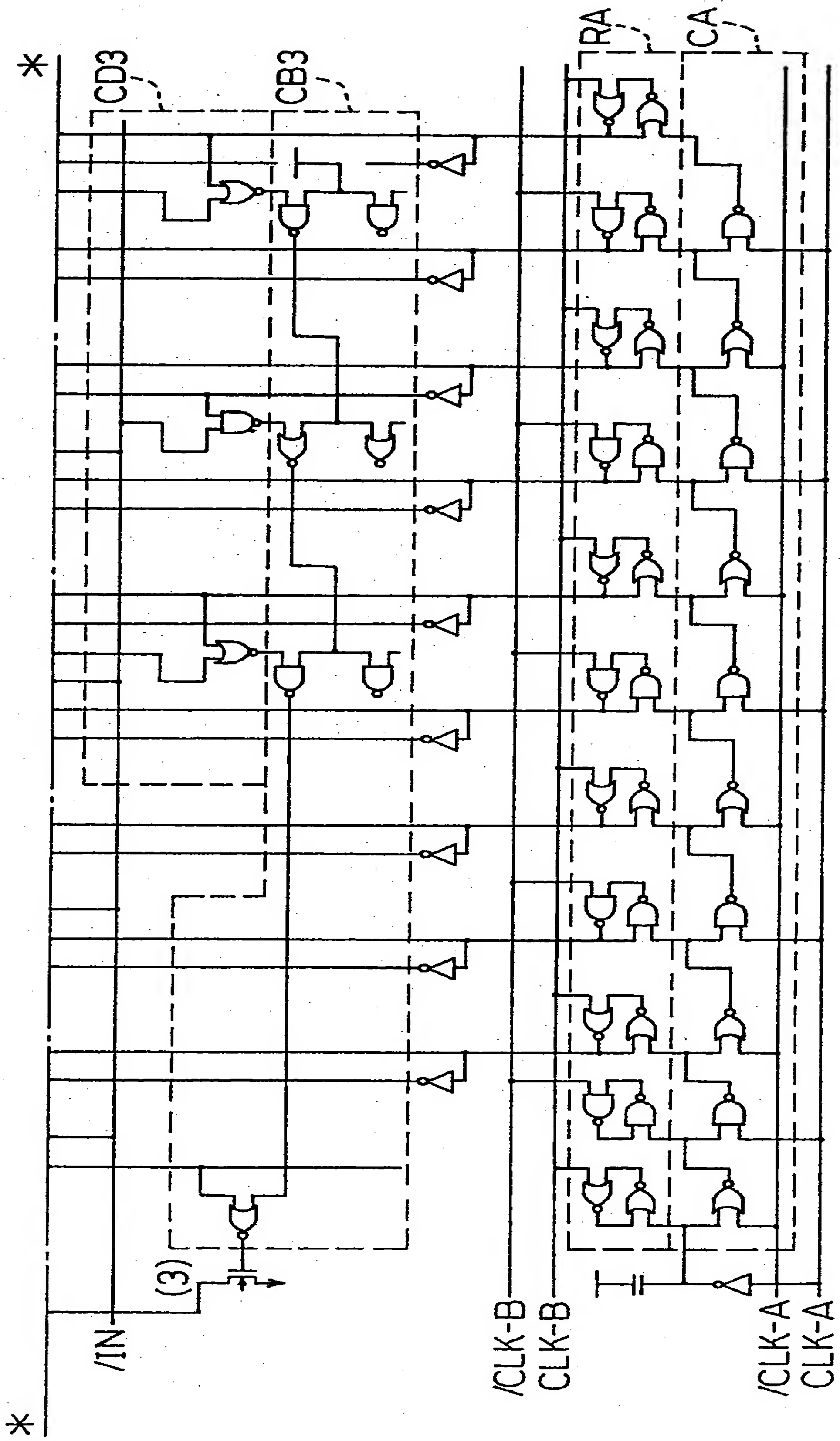


Fig. 52B



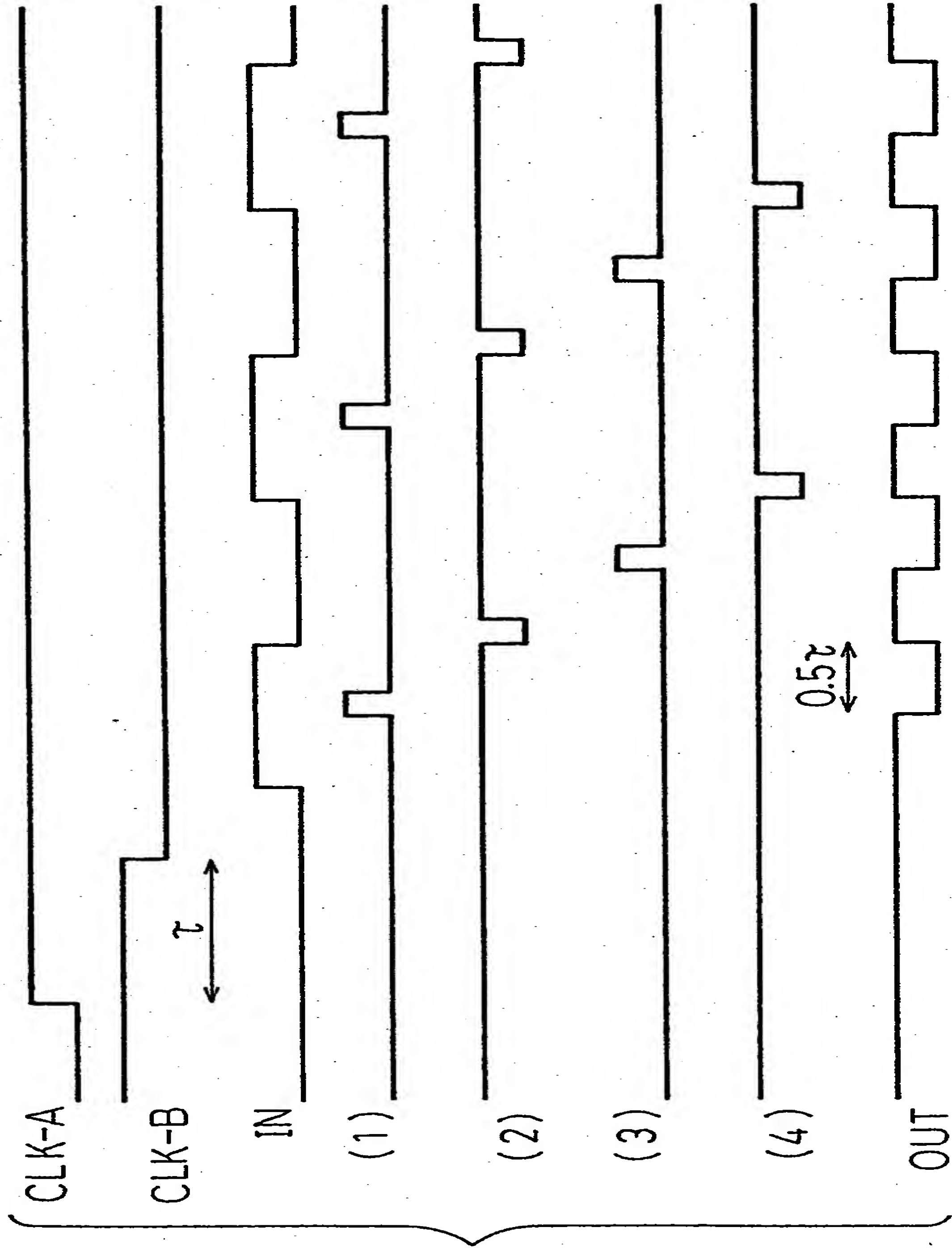


Fig. 53

Fig. 54A

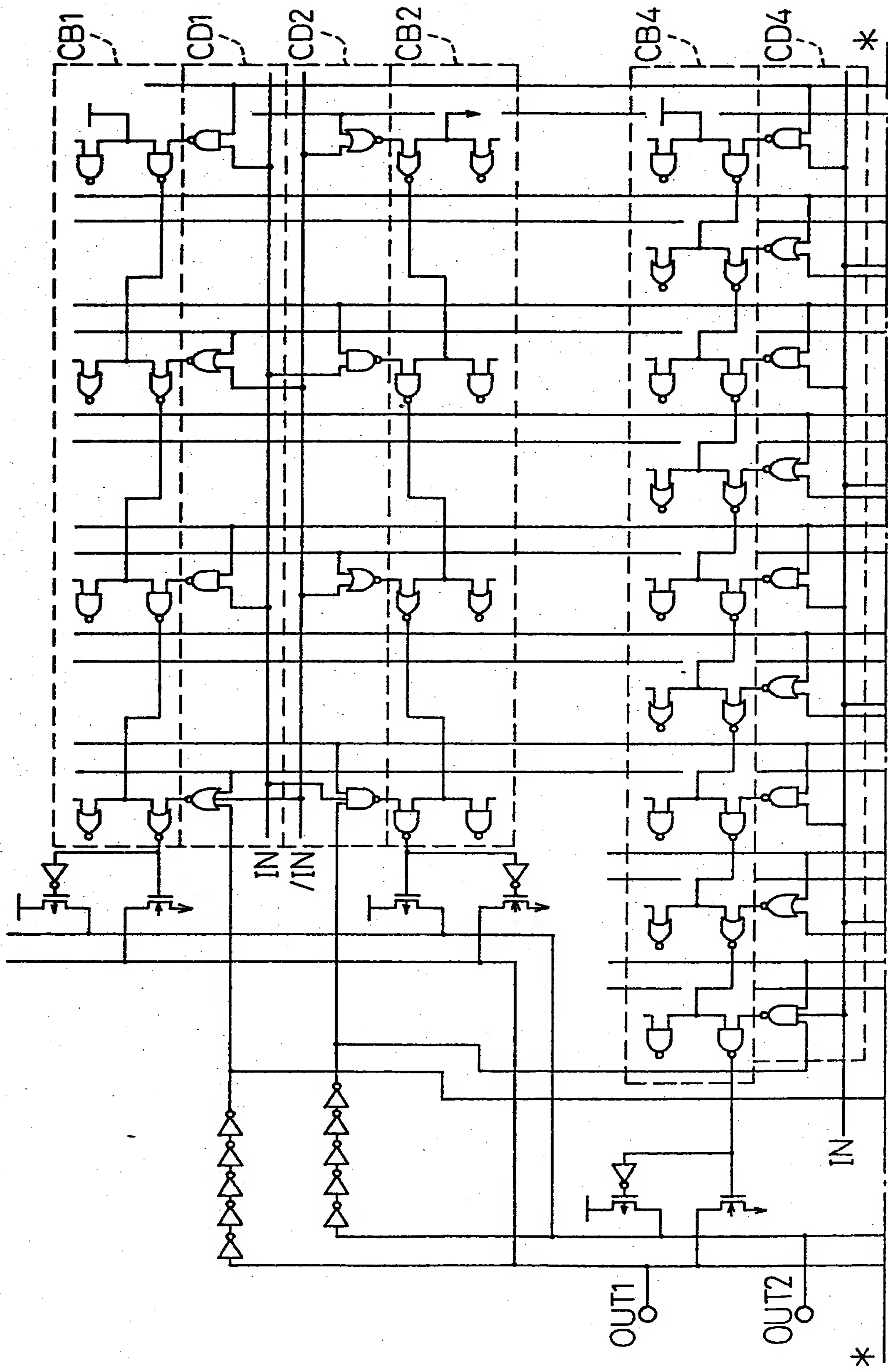
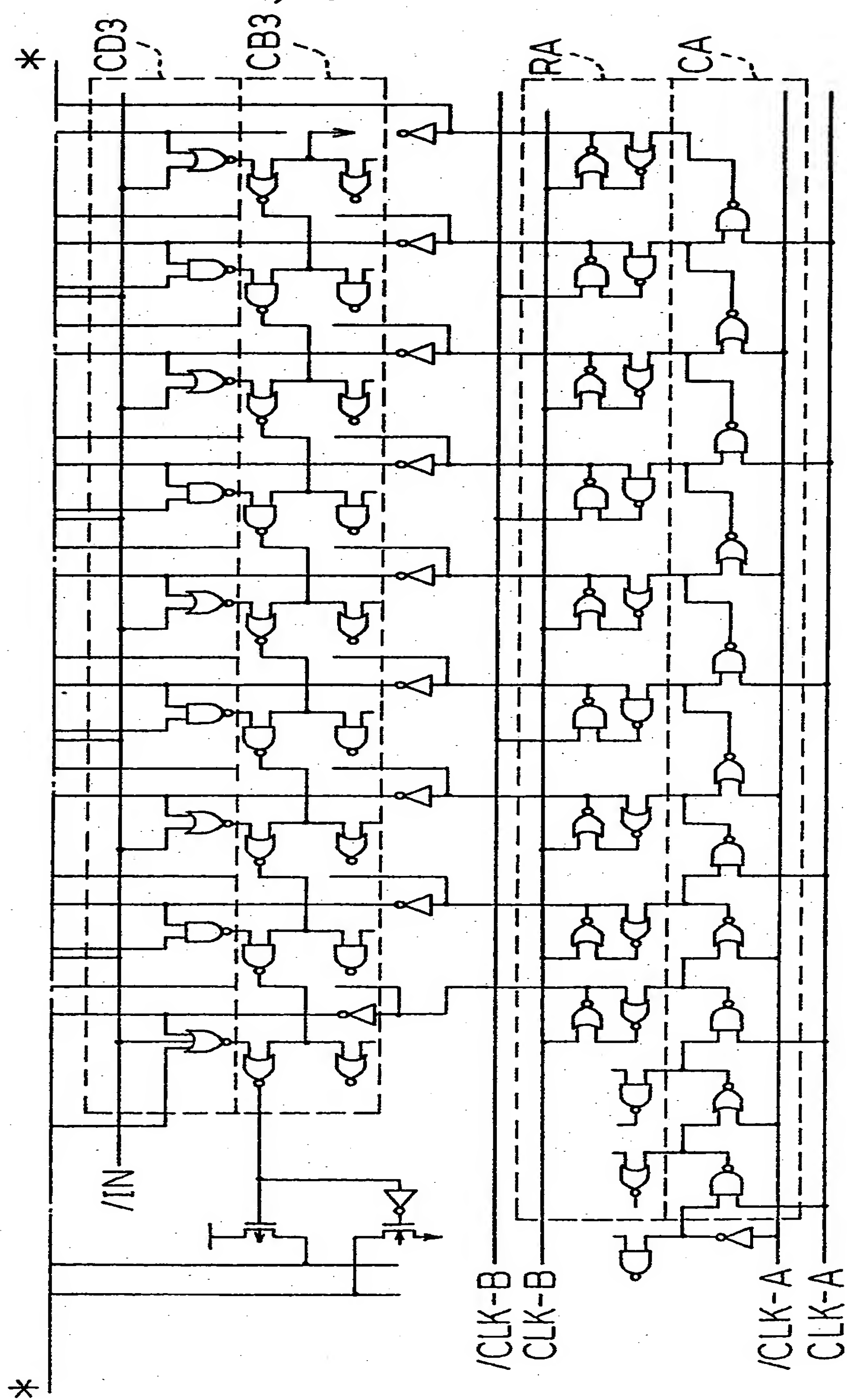


Fig. 54B



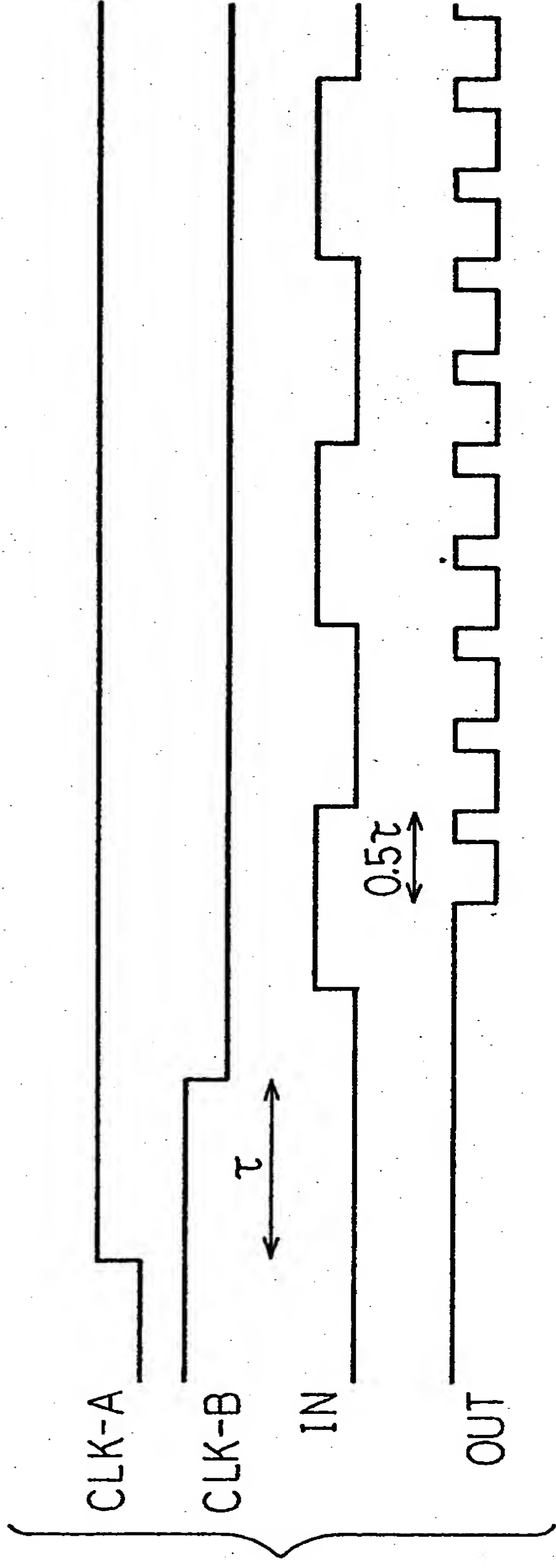


Fig.55

Fig. 56 A

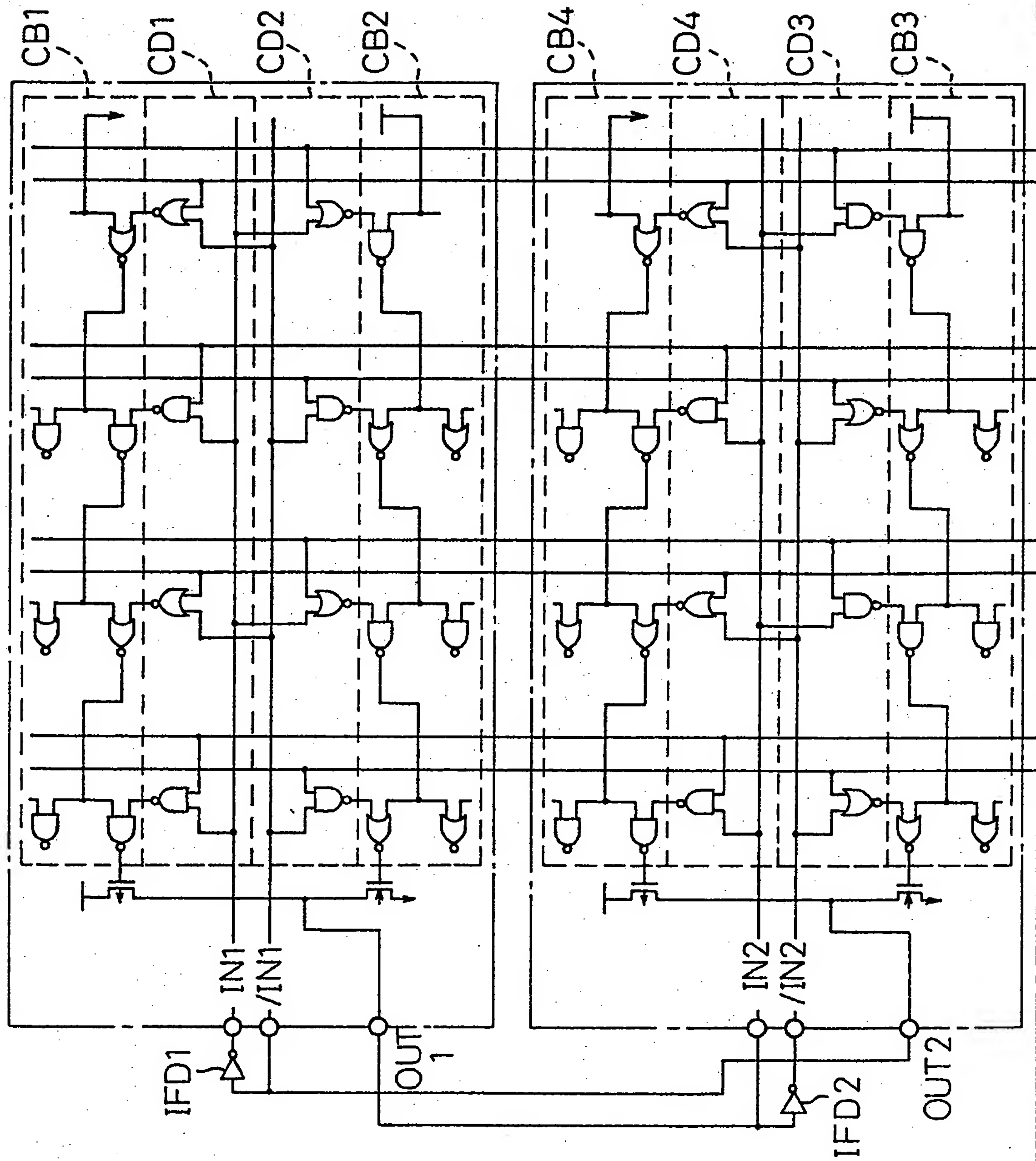
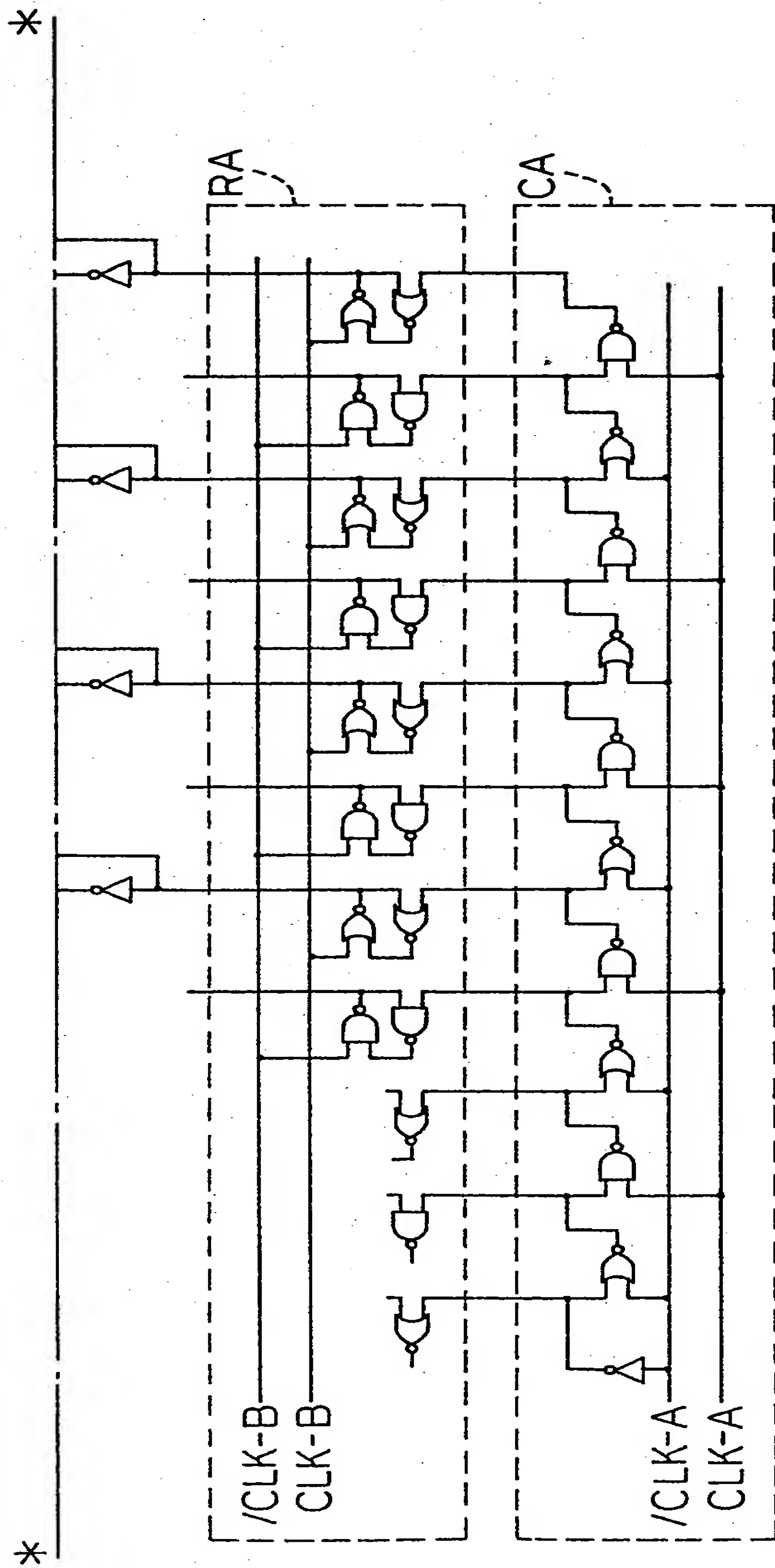


Fig. 56B



Timing diagram for a 2-to-4 decoder. The diagram shows two clock signals, CLK-A and CLK-B, and four output signals, OUT1, OUT2, OUT3, and OUT4. The period of the clock signals is labeled as T .

CLK-A and CLK-B are square wave signals. CLK-A has a period of T and a duty cycle of 50%. CLK-B has a period of T and a duty cycle of 50%, and is phase-shifted by $T/4$ relative to CLK-A.

The output signals are:

- OUT1: Active-low signal. It is high for $0.5T$ and low for $0.5T$. The period is T .
- OUT2: Active-low signal. It is high for $0.5T$ and low for $0.5T$. The period is T .
- OUT3: Active-high signal. It is low for $0.5T$ and high for $0.5T$. The period is T .
- OUT4: Active-high signal. It is low for $0.5T$ and high for $0.5T$. The period is T .

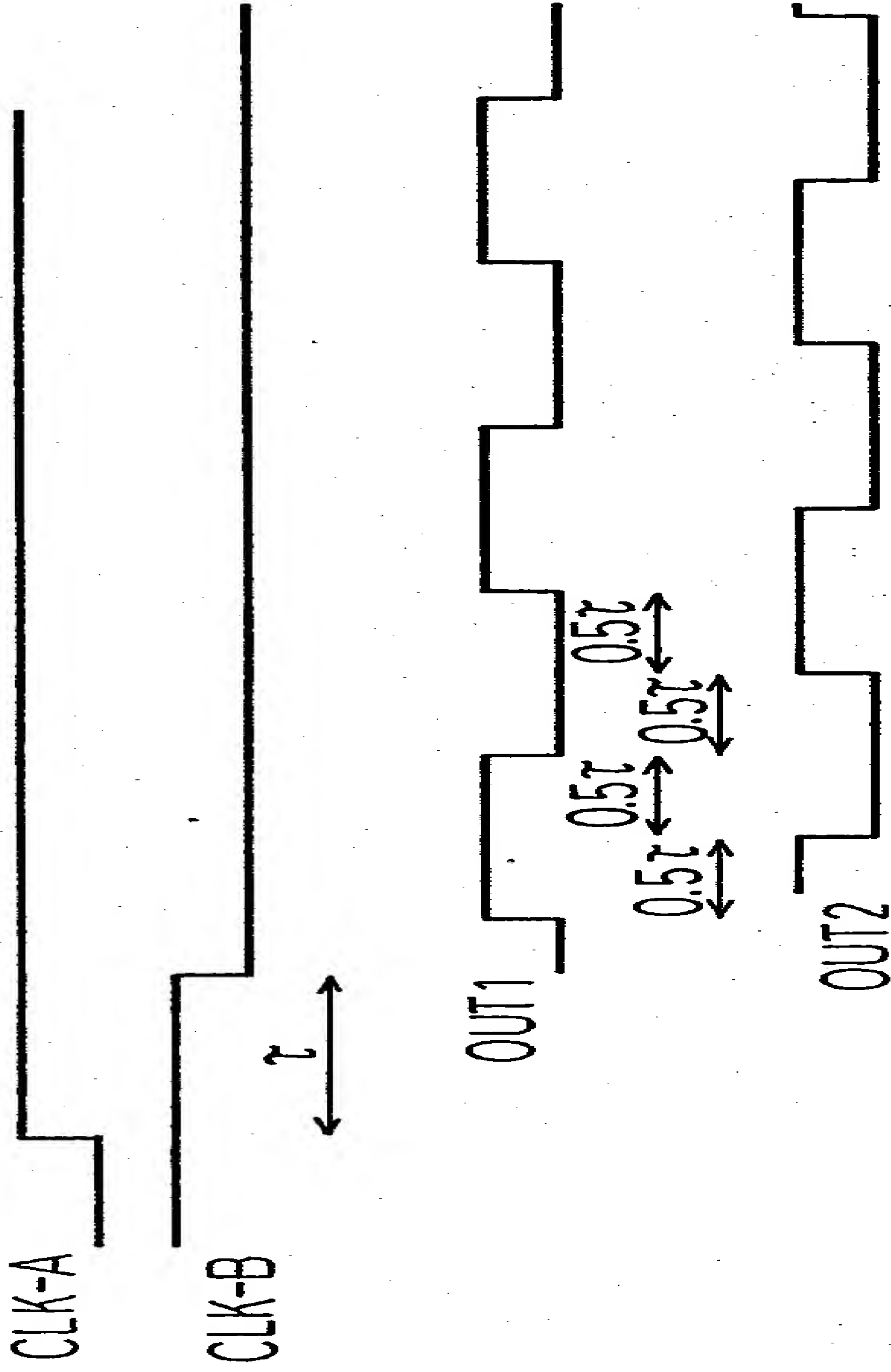


Fig:58A

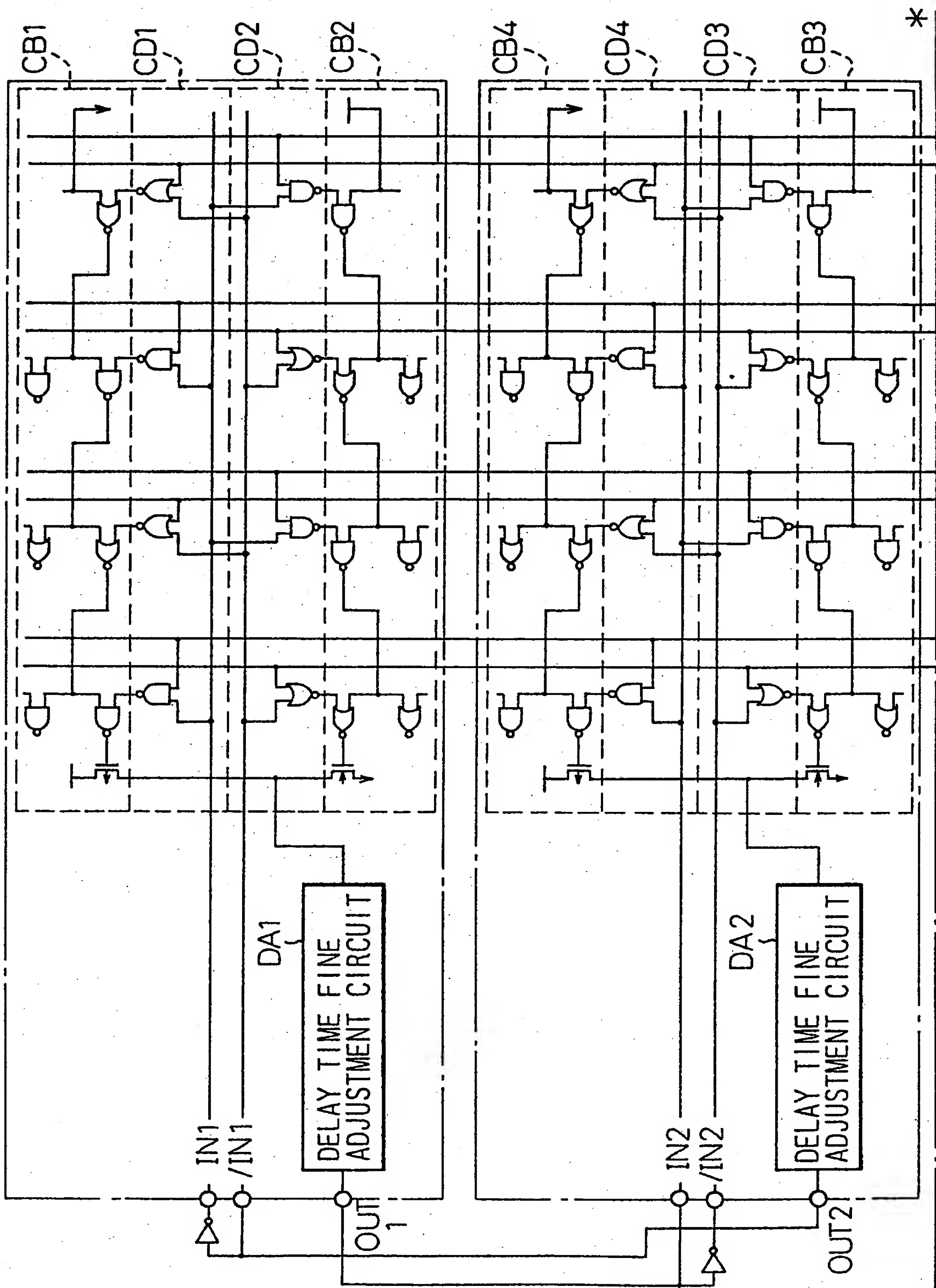


Fig. 58B

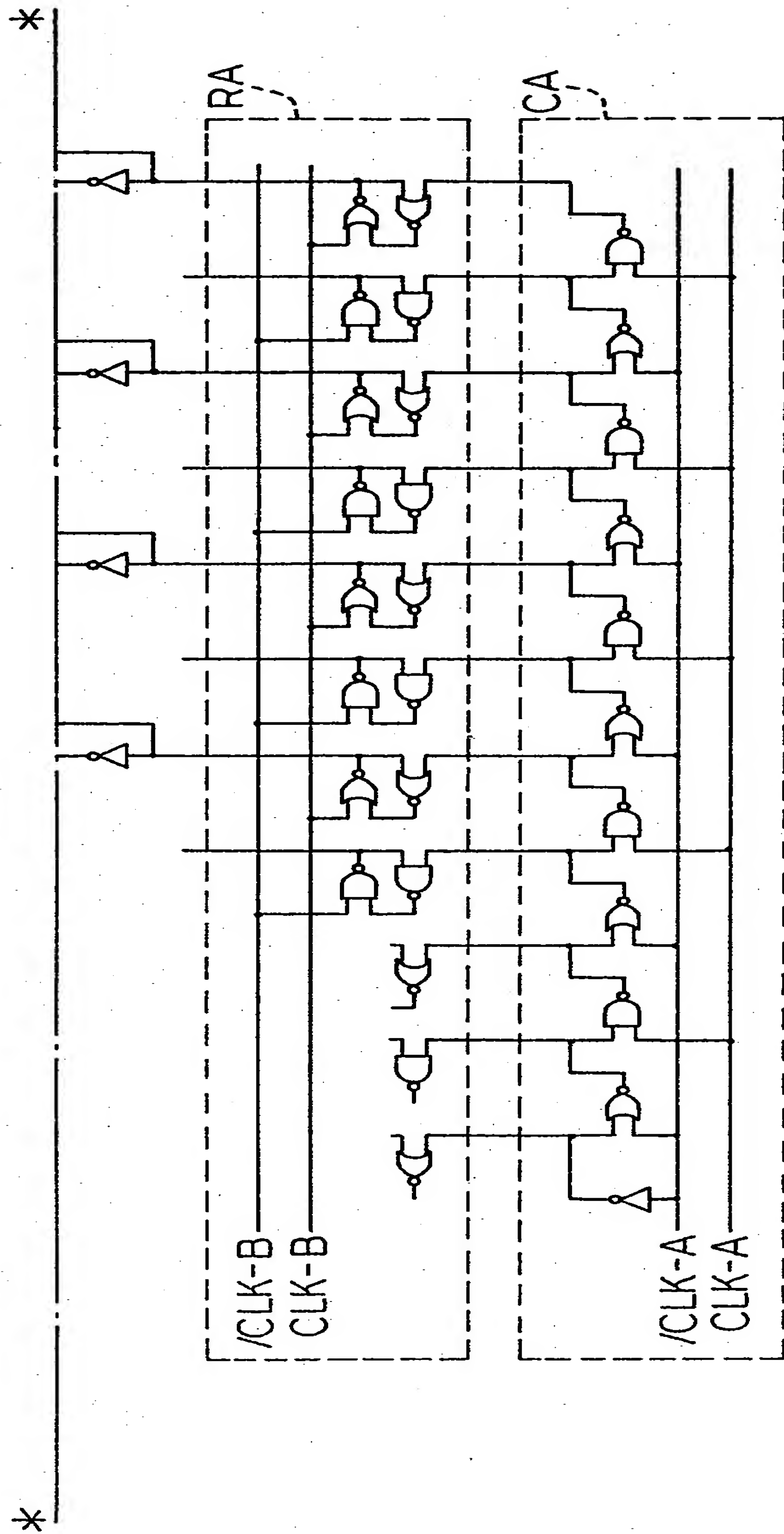


Fig.59

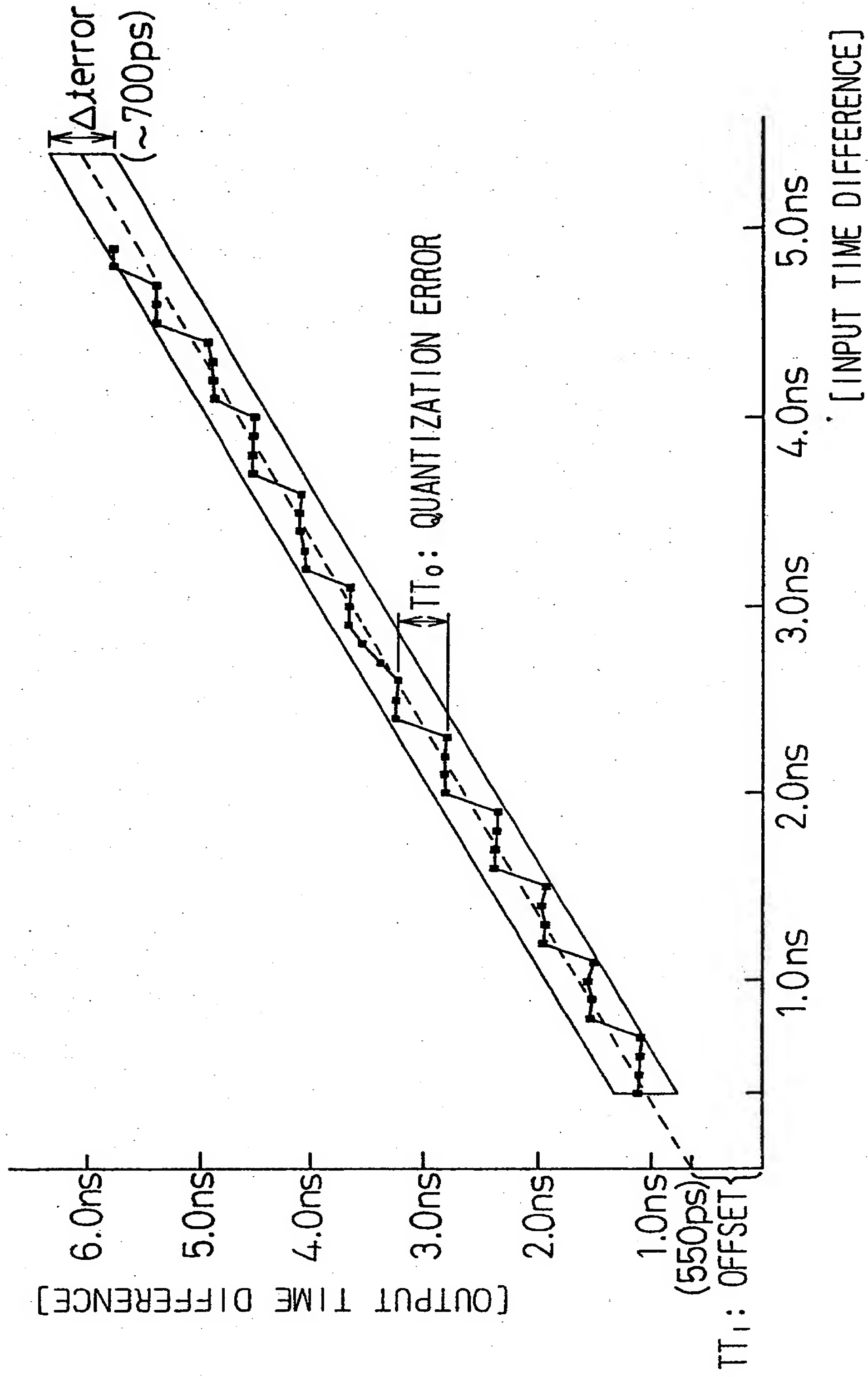


Fig. 60

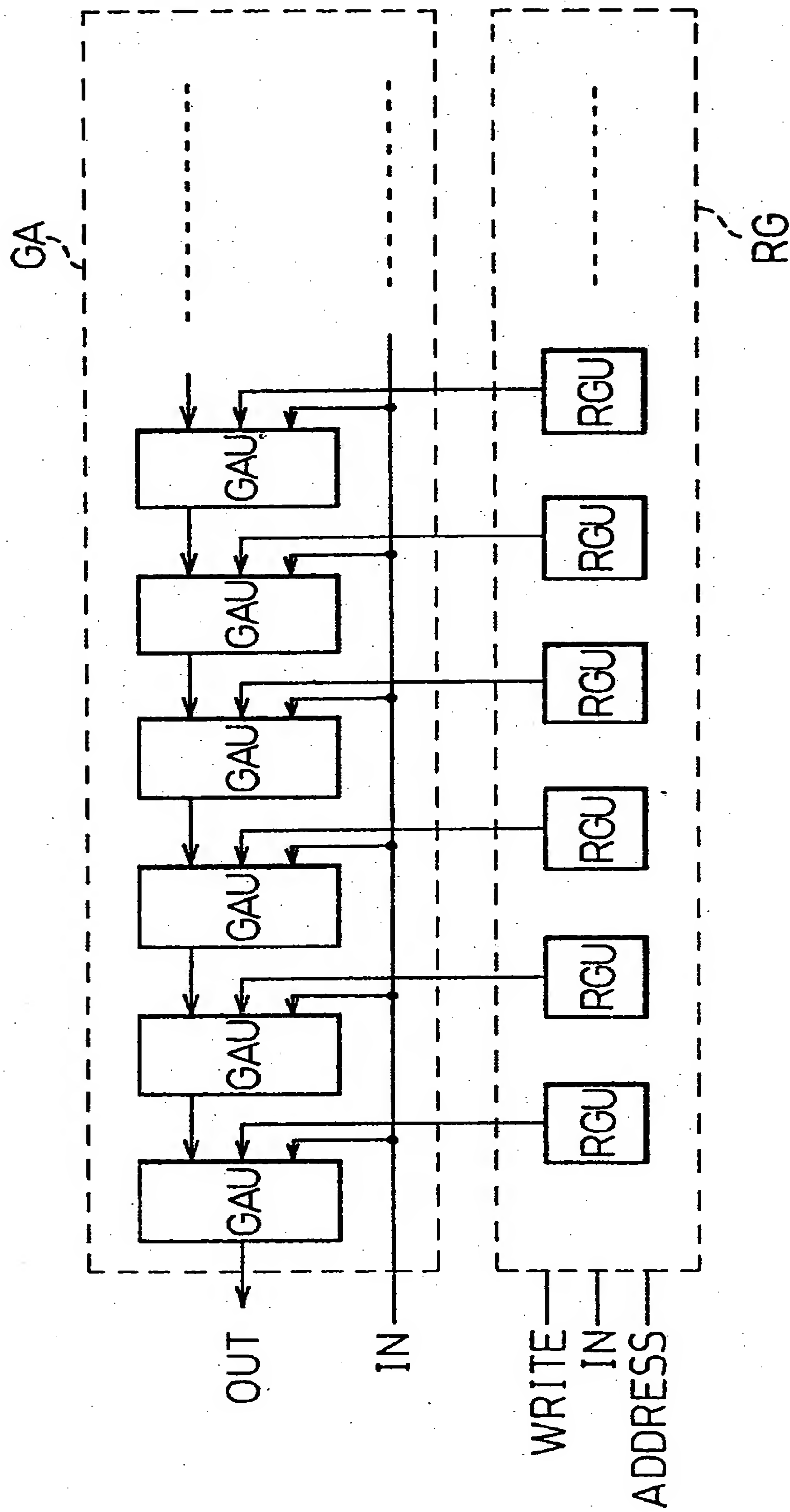


Fig. 61

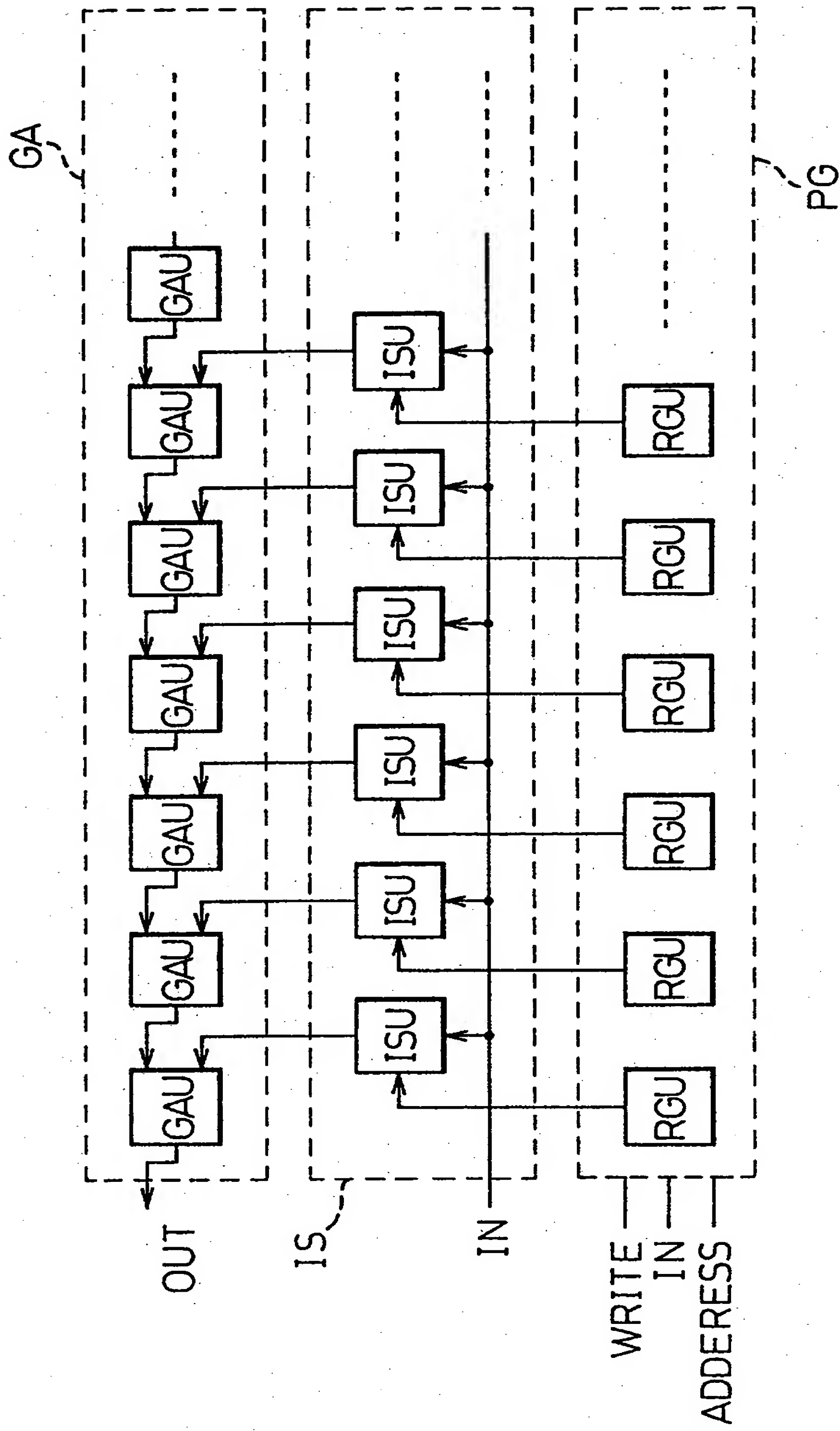
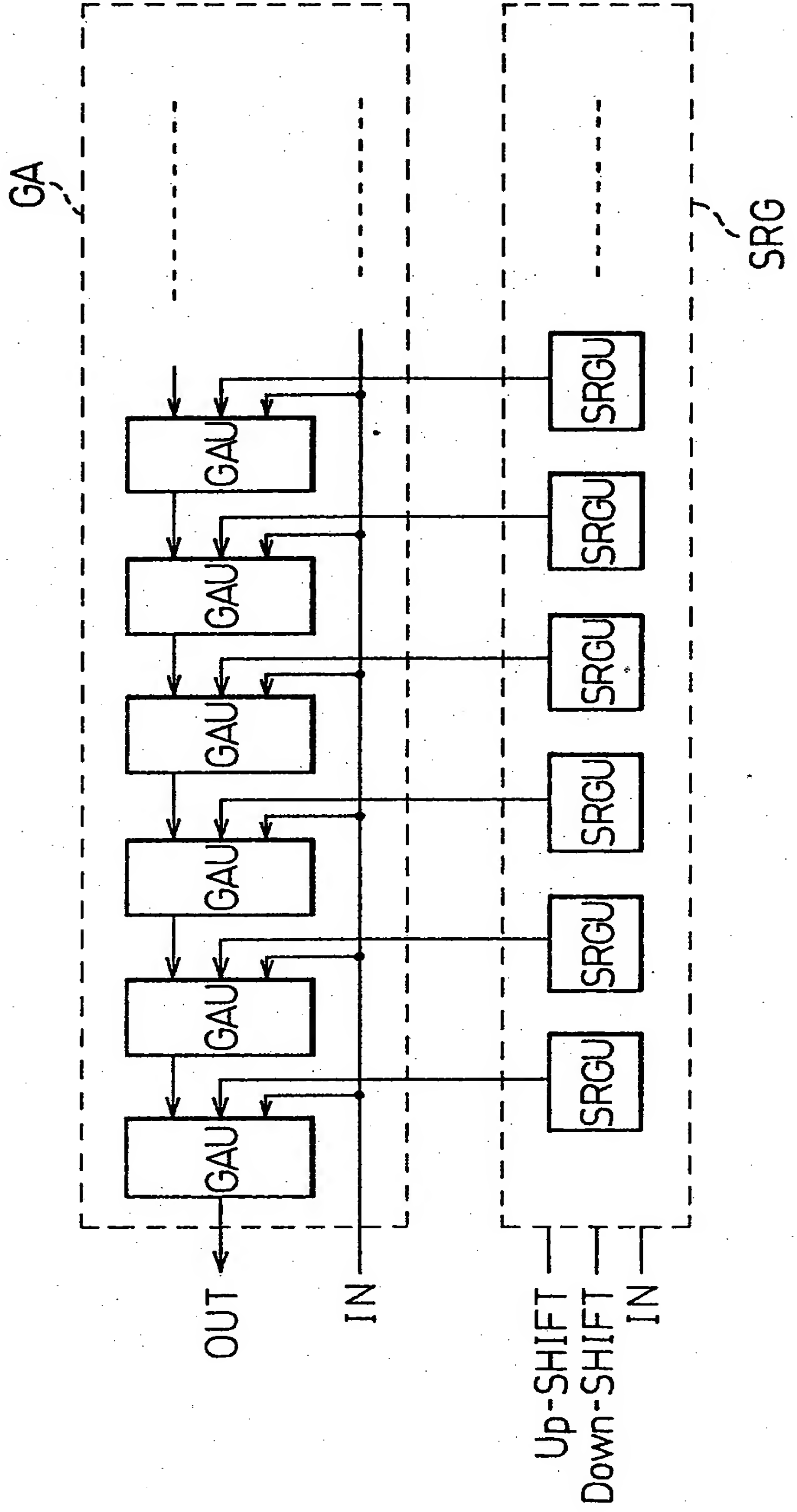


Fig. 62



Fi. 63

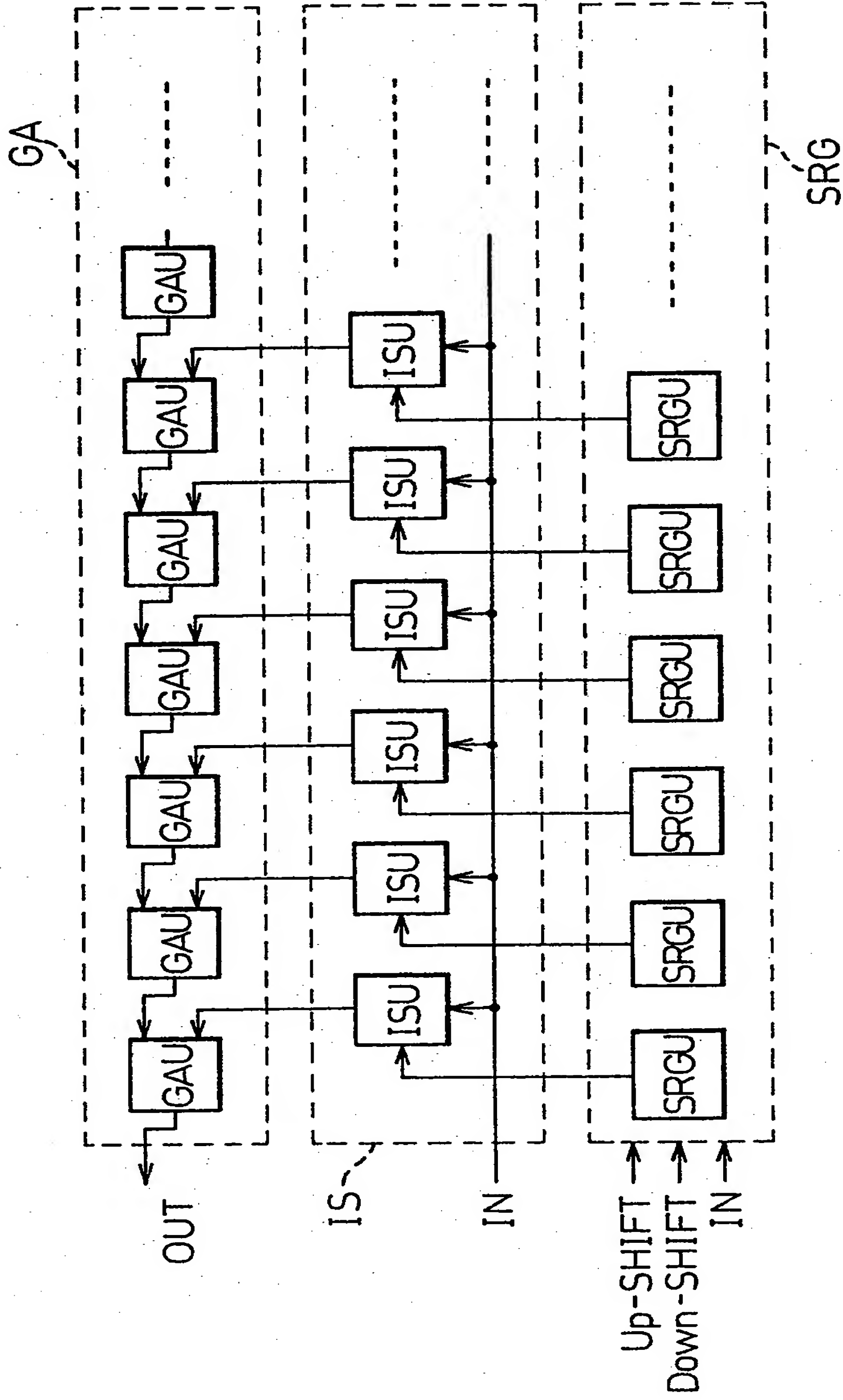


Fig. 79.

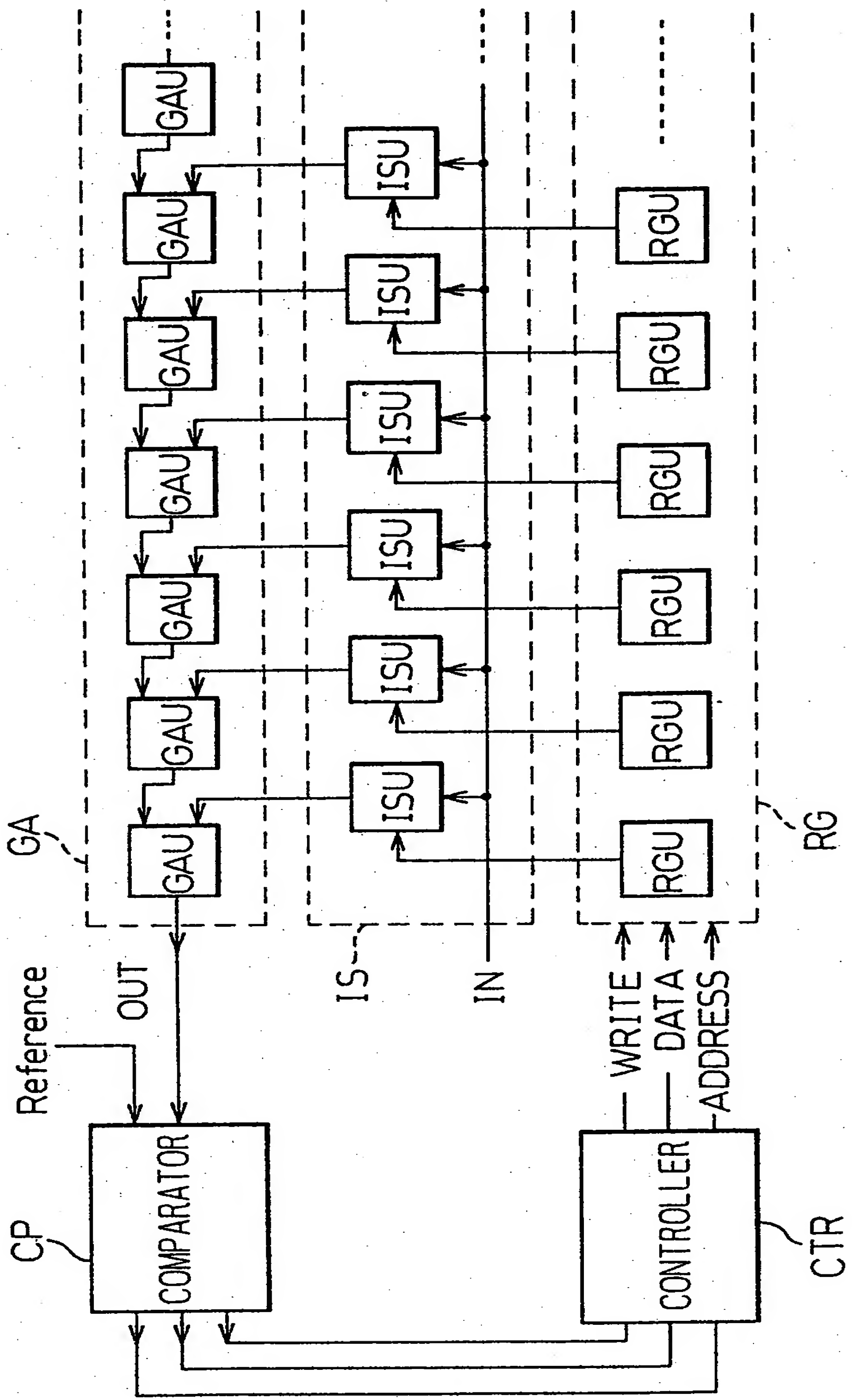


Fig. 65

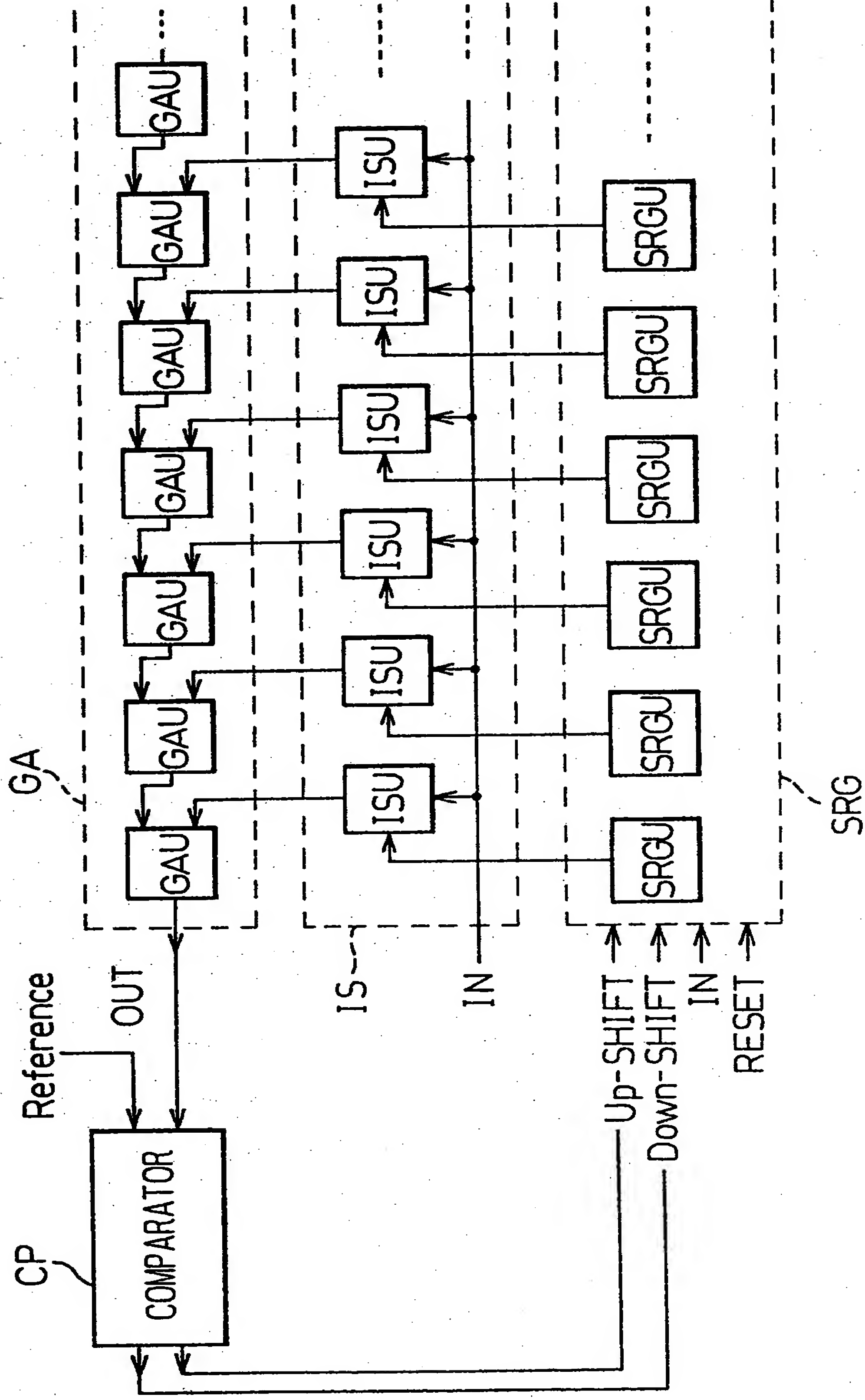


Fig. 66A

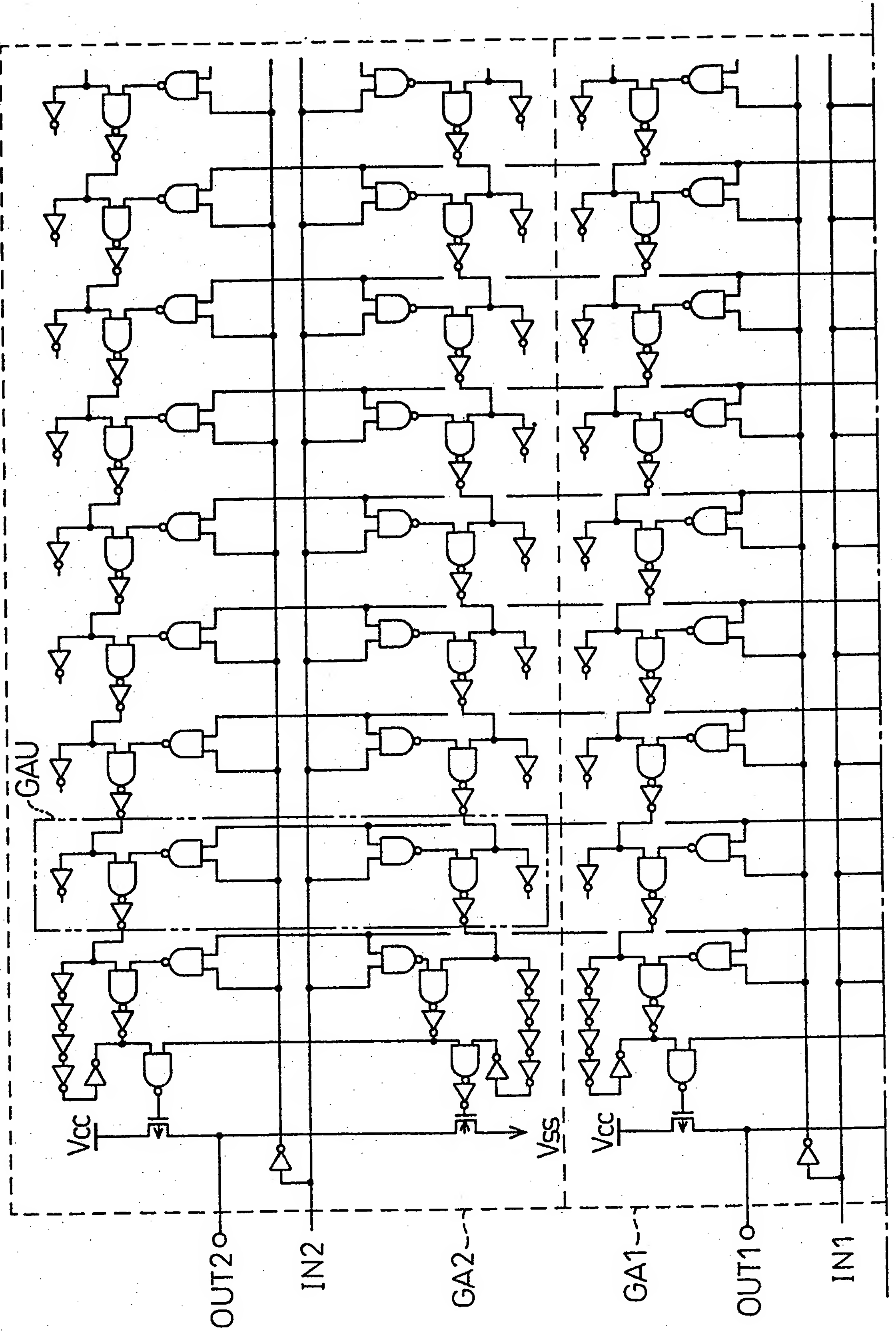


Fig. 66B

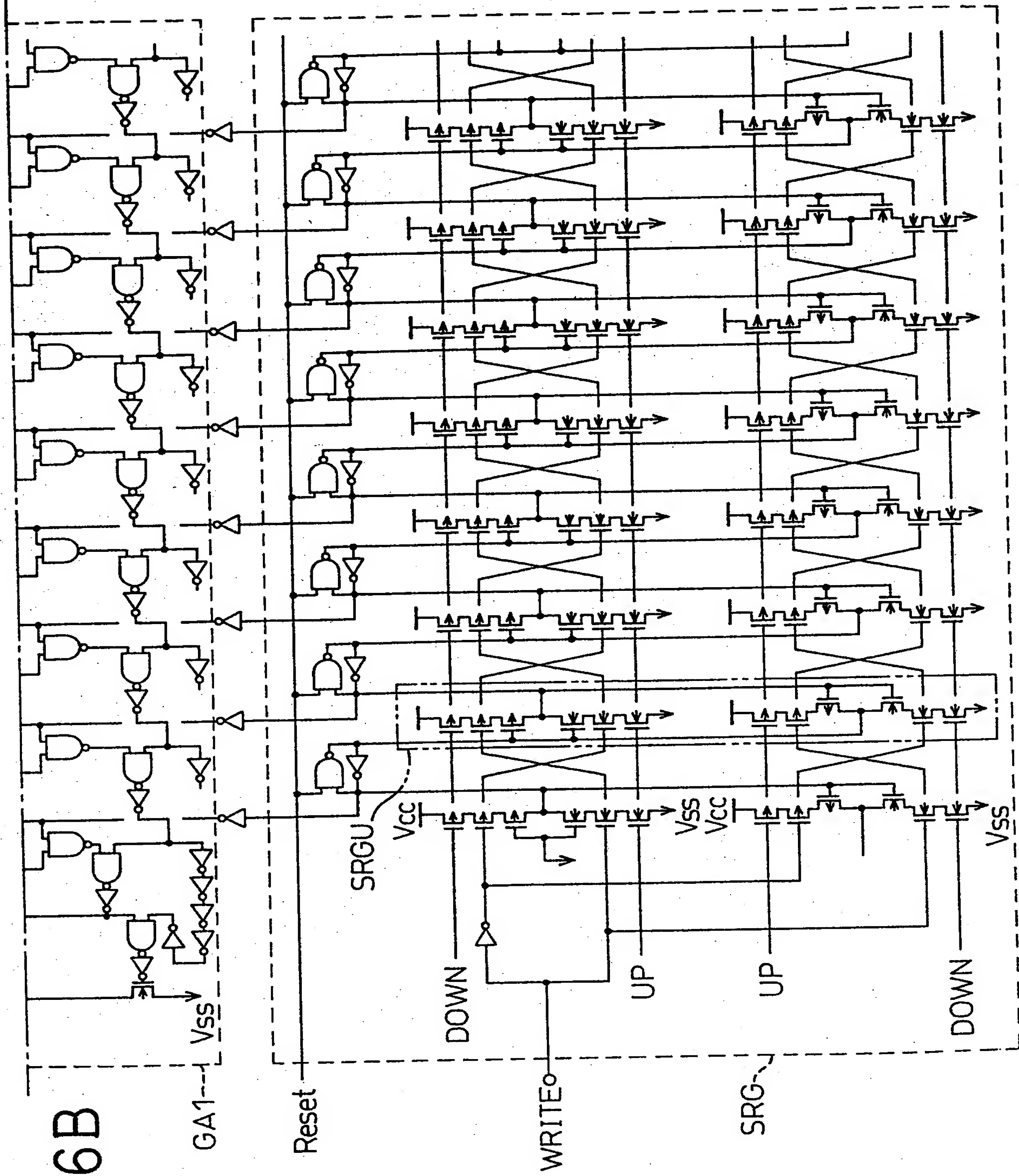


Fig. 67

